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  - L3: (13) "Reid Jonathan D$".in.
  - L4: (6) 13 not 11
  - L5: (8) "Hawkins Jeffrey A$".in.
  - L6: (8) 15 not (11 or 13)
  - L7: (1) "Kalakkad Dinesh S$".in.
  - L8: (51) "Mayer Steven T$".in.
  - L9: (48) 18 not (11 or 13 or 15 or 17)
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  - L2: (3446) clamshell
  - L3: (11) 11 and 12
  - L4: (115685) cone
  - L5: (134549) cup
  - L6: (56) 12 and 14 and 15
  - L7: (8) 16 and 11
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| 1 | ☑ | ☐ | ☐ | ☐ | US 20020108862 A1 | 20020815 | 13 | Electroplating apparatus with vertical electrical | 205/157 | 204/242 | | Fluegel, James Edward et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 2 | ☑ | ☐ | ☐ | ☐ | US 6627052 B2 | 20030930 | | Electroplating apparatus with vertical electrical | 204/224R | 204/279 | | Fluegel, James Edward et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 3 | ☑ | ☐ | ☐ | ☐ | US 6193859 B1 | 20010227 | | Electric potential shaping apparatus for holding a | 204/224R | 204/279 | | Contolini, Robert J. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 4 | ☑ | ☐ | ☐ | ☐ | US 6179983 B1 | 20010130 | | Method and apparatus for treating surface including | 205/96 | 204/227; 204/228.1; | | Reid, Jonathan David et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 5 | ☑ | ☐ | ☐ | ☐ | US 6162344 A | 20001219 | | Method of electroplating semiconductor wafer using | 205/157 | 205/96 | | Reid, Jonathan D. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 6 | ☑ | ☐ | ☐ | ☐ | US 6126798 A | 20001003 | | Electroplating anode including membrane partition | 205/143 | 204/199; 204/212; | | Reid, Jonathan David et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 7 | ☑ | ☐ | ☐ | ☐ | US 6110346 A | 20000829 | | Method of electroplating semicoductor wafer using | 205/157 | 205/137; 205/159; | | Reid, Jonathan D. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 8 | ☑ | ☐ | ☐ | ☐ | US 6074544 A | 20000613 | | Method of electroplating semiconductor wafer using | 205/157 | 205/105; 205/159 | | Reid, Jonathan D. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |

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EAST Browser - L26: (686) 25 not 24 | US 6267860 B1 | Tag: S | Doc: 73/686 (SORTED) | Format : KWIC

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| 67 | US 6280598 B1 | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 68 | US 6280597 B1 | 23 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 69 | US 6274022 B1 | 8 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 70 | US 6274021 B1 | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 71 | US 6270645 B1 | 11 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 72 | US 6267861 B1 | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 73 | US 6267860 B1 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6267860

DOCUMENT-IDENTIFIER: US 6267860 B1
**See image for Certificate of Correction**

TITLE: Method and apparatus for electroplating

---------- KWIC ---------

Assistant Examiner - XA (1):
Leader; William T.

Current US Original Classification - CCOR (1):
205/96

US 6,267,860 B1

3

In a preferred arrangement, the plating rack is capable of accommodating multiple flexible circuits that each contain multiple parts. The flex circuits were arranged in rows. The power conductive members (15, 14, respectively) ran vertically at each edge of the rack and horizontally above and below each row of parts, per the referenced disclosure. Contacts from the conductive members to the flexible circuits are positioned along the edge of the circuits section, two contacts per edge for a total of six contacts per horizontal conductive member.

During the electrical modeling of this structure a disparity in plating current was found between the contact located at the junction of the top most horizontal conductive member to vertical conductive member contact position and the center circuit section on the bottom horizontal conductive member. More current was passing through the top horizontal conductive member contacts than the bottom horizontal conductive member. Since the plating thickness is a function of the amount of electrical charge passed, the plating thickness in the locations of higher current flow will be thicker. This is so even though the core 14, 15 is preferably of sufficient size to provide substantially resistance free conduction of high plating currents for reducing plating non-uniformity when using a plurality of second openings 18. The conductive members 14, 15 are preferably of sufficient size to provide substantially resistance-free conduction of high plating currents, similar to conductive members used in other portions of an electroplating system.

Shown in FIGS. 4A and 4B are a second contact structure. In FIG. 4A, the structure is shown assembled to a workpiece 50 and in FIG. 4B the structure is shown in an exploded view to make the individual components more visible. As shown in FIG. 4A the supporting structure 10 and core 15 with insulative surface 12 has an opening 18 exposing an area 29 of core 15. An electrical contact 33 is positioned such as to make a first electrical contact with workpiece 50, and a second electrical contact 32 is provided to make electrical contact with 15 through area 29.

Workpiece 50 may be a circuitized or uncircultized substrate, a circuit board, or any other object on which one wishes to add or remove material by electroplating including noble metal plating and/or adding dendrites. Electrical contact 33 may have dendrites or other engineered surface treatments on its surface 22 for better electrical contact where it comes in contact with workpiece 50 as shown in FIG. 4B. Electrically insulative gasket 24 is positioned about contact 33 and provides a seal to prevent electroplating fluid from contacting it when the contact 33 is making electrical connection to the workpiece 50. Various methods are possible for bringing the electrical contact 33 into electrical connection with workpiece 50. For example, various spring arrangements or a thumb screw arrangement 26 as shown in FIG. 4A can be used with a spring member 34 and a resilient material 36 to assist in holding workpiece 50 in contact with electrical contact 32. Thumb screw arrangement 26 or other means for affecting the normal force contact between contact 33 and workpiece 50 would typically be electrically isolated from conducting cores 14 and 15. Insulative gasket 24 may be made of any electrically insulative material but is preferably an elastomer material such as VITON™ and is preferably in contact with workpiece 50 and contact 33 as shown in FIG. 4A. VITON is a trademark of E.I. du Pont de Nemours & Co., Inc. The insulative gasket may also be made inflatable as a way to bring it into contact with contact 33 and workpiece 50.

In accordance with the present invention, a resistor is provided between electrical conductive members 14, 15 and

4

the workpiece 50. In the arrangement disclosed herein, electrical contact 33 can act as the resistor, also referred to herein as the dropping resistance. In previous arrangements, the size of electrical contacts to the workpiece was maximized and the material resistivity was minimized believing a minimum total resistance between the workpiece and power distribution would provide the most uniform plating.

In accordance with the present invention, the ratio of the dropping resistance to the conductive member resistance is typically at least 10:1, more typically about 10:1 to about 50:1 and preferably about 20:1 to about 40:1. The conductive member resistance is the maximum resistance from one second contact 32 (see FIGS. 4A and 4B) to another second contact 32 which are positioned within openings 18 of FIG. 3. The resistance of the resistor 33 is determined by the resistivity of the material used and its dimensions. The electrical resistance of a conductor of uniform cross-section is the resistivity of the material multiplied by the conductor length divided by the cross-sectional area using consistent units. Resistors 33 are typically made of copper, brass, titanium, nickel and stainless steel. Copper has a resistivity of about 1.8 E$^{-8}$ ohm meters, brass has a resistivity of about 18 E$^{-8}$ ohm meters, titanium has a resistivity of about 42 E$^{-8}$ ohm meters and stainless steel has a resistivity in the range of 50–70 E$^{-8}$ ohm meters. Accordingly, use of a material having a higher resistivity can provide a higher resistance using the same physical dimensions as a lower resistivity material. Maintaining the physical size of the electrical contact 33 by increasing the material resistivity instead of the physical size of the contacts makes it possible to use existing plating equipment while implementing the present invention.

It is preferred that the material employed have a resistivity of at least about 15 E$^{-8}$ ohm meters and more preferably at least about 20 E$^{-8}$ ohm meters. Preferred materials include brass, titanium and stainless steel and more preferably titanium due to its resistivity and being generally chemically inert in the plating baths employed. In addition, the resistor is preferably relatively inert in the plating process. The addition of these dropping resistors does not actually use additional electrical power of the plating process because the plating baths are normally heated, the relatively small amount of power dissipated by the resistors of the present invention will contribute to the bath heating replacing electrical power consumed by the heaters. Since the power dissipated by the dropping resistors are proportional to the current passed, this can be accounted for when setting up a new part or changing the part plating thickness by adjusting the plating parameters.

FIGS. 1 and 2 are graphs for two different plating racks illustrating current distribution range across the rack in percent versus ratio of dropping resistor to bus bar. In FIG. 1, the vertical conductive members have cross-sections of 1.5 by 1 inch and horizontal conductive members of 0.3 inch by 1 inch. In FIG. 2, the vertical conductive members have cross-sections of 1.5 by 1 inch and horizontal conductive members of 1.5 inch by 1 inch. As illustrated in FIGS. 1 and 2, the ratio of dropping resistor to conductive member resistances is typically at least about 10:1 to provide distribution range across the plating rack. In particular, the inherent current non-uniformity for the design analyzed can be as high as 15% without dropping resistors or be reduced to less than 1% depending on the magnitude of the dropping resistor.

FIGS. 1 and 2 show the effect of this dropping resistor on the plating current ratio across the plating rack and workpieces mounted thereon, that a dropping resistor of only

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Ti = 154 20 milliohm
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| 67 | US 6280598 B1 | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 68 | US 6280597 B1 | 23 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 69 | US 6274022 B1 | 8 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 70 | US 6274021 B1 | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 71 | US 6270645 B1 | 11 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 72 | US 6267861 B1 | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 73 | US 6267860 B1 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6267860

DOCUMENT-IDENTIFIER: US 6267860 B1
**See image for Certificate of Correction**

TITLE: Method and apparatus for electroplating

---------- KWIC ---------

Assistant Examiner - XA (1):
Leader; William T.

Current US Original Classification - CCOR (1):
205/96

(12) **United States Patent**
**Brodsky**

(10) **Patent No.: US 6,267,860 B1**
(45) **Date of Patent: Jul. 31, 2001**

(54) **METHOD AND APPARATUS FOR ELECTROPLATING**

(75) Inventor: **William Louis Brodsky**, Binghamton, NY (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/361,728**

(22) Filed: **Jul. 27, 1999**

(51) **Int. Cl.**[7] .......... **C25D 17/04**

(52) **U.S. Cl.** .......... 205/96; 204/230.2; 204/297.06; 204/297.1; 204/297.13; 204/DIG. 7

(58) **Field of Search** .......... 205/96; 204/230.2, 204/297.1, 297.06, 297.13, 297.15, DIG. 7

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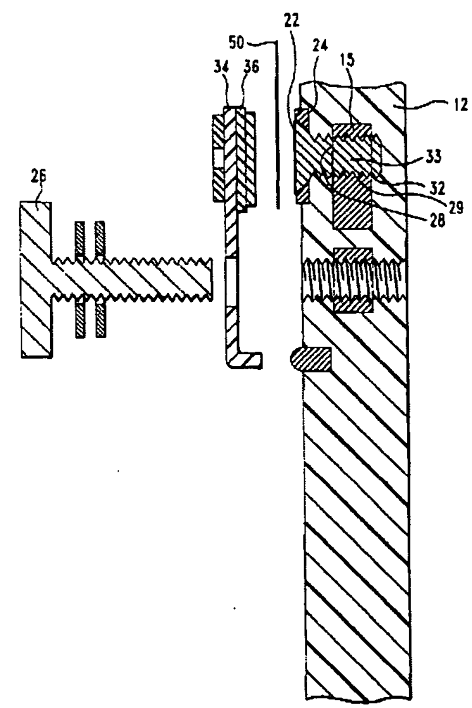
*Primary Examiner*—Kathryn Gorgos
*Assistant Examiner*—William T. Leader
(74) *Attorney, Agent, or Firm*—Connolly, Bove, Lodge & Hutz, LLP.; Lawrence R. Fraley, Esq.

(57) **ABSTRACT**

Electrolytic plating of a workpiece is enhanced by providing a resistor between the workpiece and electrically conductive support member.

**19 Claims, 6 Drawing Sheets**



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| 2 | US 6193859 B1 | 21 | | | | | | | ☑ | | | | USPAT |
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| 6 | US 6110346 A | 8 | | | | | | | ☑ | | | | USPAT |
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| 8 | US 20020108862 A | 13 | | | | | | | ☑ | | | | US-PG |

US-PAT-NO: 6193859

DOCUMENT-IDENTIFIER: US 6193859 B1

TITLE: Electric potential shaping apparatus for holding a semiconductor wafer during electroplating

---------- KWIC ---------

Brief Summary Text - BSTX (11):
In accordance with the present invention, an apparatus for depositing an electrically conductive layer on the surface of a substrate such as a wafer comprises a flange. The flange has a cylindrical wall and an annulus extending inward from the cylindrical wall, the annulus having an inner perimeter which defines a flange central aperture. The apparatus also includes a cup for supporting the wafer along a peripheral region thereof. The cup has a cup central aperture defined by an inner perimeter of the cup, the cup being positioned above the flange.

Brief Summary Text - BSTX (12):
In one embodiment, the diameter of the flange central aperture is less than the diameter of the cup central aperture. The annulus of the flange thus extends under the edge region of the wafer surface and reduces the electric current flux to this edge region during electroplating. This, in turn, reduces the thickness of the deposited electrically conductive layer on the edge region of the wafer surface. Of importance, the thickness of the deposited electrically conductive layer on the edge region of the wafer surface is reduced without the use of thieves.

Brief Summary Text - BSTX (14):
The flange can further include a plurality of apertures extending through the cylindrical wall of the flange. By locating these apertures adjacent the cup and near the edge region of the wafer surface, air bubbles entrapped on the wafer surface can readily escape through the apertures. To further enhance removal of entrapped air bubbles, the wafer can be rotated while the plating solution is directed towards the center of the wafer surface.

Brief Summary Text - BSTX (16):
In accordance with another embodiment of the present invention, a method of depositing an electrically conductive layer on the wafer surface includes providing a cup attached to a flange, the cup having an inner perimeter which defines a cup central aperture, the flange having an annulus. The wafer is then mounted in the cup so that the wafer surface is exposed through the cup central aperture. The cup and flange are then placed into a plating solution, the plating solution contacting the wafer surface. An electrical field and electric current flux is then produced between the wafer surface and an anode in the plating solution wherein the annulus of the flange shapes the electric current flux and reduces the thickness of the deposited electrically conductive layer on the edge region of the wafer surface.

Drawing Description Text - DRTX (3):

(12) United States Patent
Contolini et al.

(10) Patent No.: US 6,193,859 B1
(45) Date of Patent: Feb. 27, 2001

(54) ELECTRIC POTENTIAL SHAPING APPARATUS FOR HOLDING A SEMICONDUCTOR WAFER DURING ELECTROPLATING

(75) Inventors: Robert J. Contolini, Lake Oswego; Jonathan Reid, Sherwood; Evan Patton, Portland; Jingbin Feng, Tigard; Steve Taatjes, West Linn, all of OR (US); John Owen Dukovic, Pleasantville, NY (US)

(73) Assignees: Novellus Systems, Inc., San Jose, CA (US); International Business Machines Corporation, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/074,624

(22) Filed: May 7, 1998

Related U.S. Application Data

(62) Division of application No. 08/970,120, filed on Nov. 13, 1997, now Pat. No. 6,159,354.

(51) Int. Cl.$^7$ .......... C25D 17/00; C25B 9/00
(52) U.S. Cl. .......... 204/224 R; 204/279
(58) Field of Search .......... 204/224 R, 212, 204/237, 279; 205/157, 96

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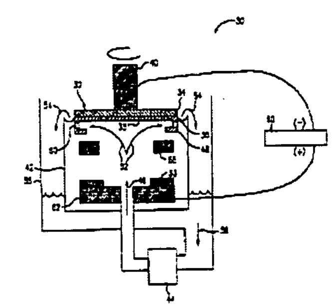
Primary Examiner—Donald R. Valentine
(74) Attorney, Agent, or Firm—Skjerven Morrill MacPherson LLP; David E. Steuber

(57) ABSTRACT

An apparatus for depositing an electrically conductive layer on the surface of a wafer comprises a flange. The flange has a cylindrical wall and an annulus attached to a first end of the cylindrical wall. The annulus shields the edge region of the wafer surface during electroplating reducing the thickness of the deposited electrically conductive layer on the edge region. Further, the cylindrical wall of the flange can be provided with a plurality of apertures adjacent the wafer allowing gas bubbles entrapped on the wafer surface to readily escape.

29 Claims, 12 Drawing Sheets



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EAST Browser - L13: (1) 11 and 9 | US 6627052 B2 | Tag: S | Doc: 1/1 (SORTED) | Format: KWIC

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| 1 | US 6627052 B2 | 10 | | | | | ☑ | | | | USPAT |

US-PAT-NO: 6627052

DOCUMENT-IDENTIFIER: US 6627052 B2

TITLE: Electroplating apparatus with vertical electrical contact

---------- KWIC ---------

Abstract Text - ABTX (1):
An electrodeposition apparatus for depositing material on a surface of a substrate. The electrodeposition apparatus includes at least one contact for vertically contacting the substrate and providing electrical connection to the substrate. The at least one contact does not scratch the surface of the substrate to be plated. A voltage source is connected to the at least one contact.

US Patent No. - PN (1):
6627052

TITLE - TI (1):
Electroplating apparatus with vertical electrical contact

Brief Summary Text - BSTX (5):
The present inventors believe that contact arrangements used in a typical electroplating apparatus cause slight imperfections on the copper (Cu) seed layer during plating. These known contact arrangements have contact points located, for example, at the ends of 128 short "arms." These arms take up compression when, eg, sealing the wafer in a "clamshell" for electroplating. See, for example, known electroplating tools such as the SABRE Electro-fill System marketed by Novellus Systems, Inc, San Jose, Calif. See, also, U.S. Pat. No. 6,074,544 (Method Of Electroplating Semiconductor Wafer Using Variable Currents And Mass Transfer To Obtain Uniform Plated Layer) and U.S. Pat. No. 6,139,712 (Method Of Depositing Metal Layer), which are both incorporated in their entireties herein by reference. When a Cu seed layer is greater than 1000 A thickness, these contacts don't pose a serious problem. However, as the industry moves to thinner and thinner seed layers, these contacts do enough damage to cause large variations in plated film thickness. Having the actual contact point located at the end of a "moment arm" induces a certain, be it slight, amount of motion in the "x" direction in order to accommodate for the "z" motion required for sealing the wafer in the clamshell for electroplating. When the movement in the "x" direction occurs, it scratches across the seed layer reducing the number of good electrical connections.

128 unit.

Brief Summary Text - BSTX (7):
The present invention provides an apparatus for depositing material, electroetching, and/or electropolishing on a surface of a substrate. The apparatus includes at least one electrical contact for contacting the substrate and providing an electrical connection to the substrate. The at least one contact is movable only in a vertical direction with respect to the substrate.

(12) United States Patent
Fluegel et al.

(10) Patent No.: US 6,627,052 B2
(45) Date of Patent: Sep. 30, 2003

(54) ELECTROPLATING APPARATUS WITH VERTICAL ELECTRICAL CONTACT

(75) Inventors: James Edward Fluegel, Rhinebeck, NY (US); Peter Stevens Locke, Hopewell Junction, NY (US); Yuet-Ying Yu, Hopewell Junction, NY (US)

(73) Assignee: International Business Machines Corporation, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/734,830

(22) Filed: Dec. 12, 2000

(65) Prior Publication Data

US 2002/0108862 A1 Aug. 15, 2002

(51) Int. Cl.$^7$ .......... C25D 17/00; C25B 9/00
(52) U.S. Cl. .......... 204/224 R; 204/279
(58) Field of Search .......... 204/224 R, 279

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Eight (8) pages of data sheets (believed dated earlier than Jul. 13, 2000) for Chomerics products.
Five (5) pages of schematics for Buckled Beam, Unbuckled Beam, Contact A Series, Contact E Series and Plungers (believed dated prior to Dec. 12, 2000).
Five (5) pages (4–29, 4–30, 1–7, 5–48 and 4–71) from Sabre manuals (believed dated earlier than Nov. 21, 2000).

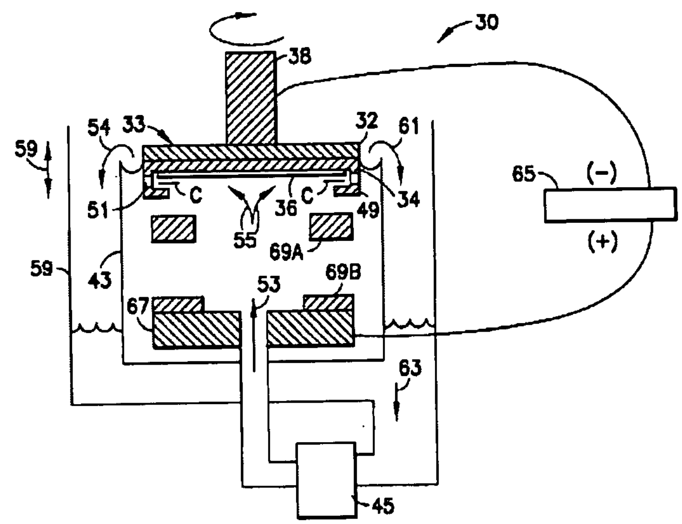
* cited by examiner

Primary Examiner—Donald R. Valentine
(74) Attorney, Agent, or Firm—Joseph P. Abate

(57) ABSTRACT

An electrodeposition apparatus for depositing material on a surface of a substrate. The electrodeposition apparatus includes at least one contact for vertically contacting the substrate and providing electrical connection to the substrate. The at least one contact does not scratch the surface of the substrate to be plated. A voltage source is connected to the at least one contact.

15 Claims, 5 Drawing Sheets

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US-PAT-NO: 6627052

DOCUMENT-IDENTIFIER: US 6627052 B2

TITLE: Electroplating apparatus with vertical electrical contact

---------- KWIC ---------

Brief Summary Text - BSTX (5):

The present inventors believe that contact arrangements used in a typical electroplating apparatus cause slight imperfections on the copper (Cu) seed layer during plating. These known contact arrangements have contact points located, for example, at the ends of 128 short "arms." These arms take up compression when, eg, sealing the wafer in a "clamshell" for electroplating. See, for example, known electroplating tools such as the SABRE Electro-fill System marketed by Novellus Systems, Inc, San Jose, Calif. See, also, U.S. Pat. No. 6,074,544 (Method Of Electroplating Semiconductor Wafer Using Variable Currents And Mass Transfer To Obtain Uniform Plated Layer) and U.S. Pat. No. 6,139,712 (Method Of Depositing Metal Layer), which are both incorporated in their entireties herein by reference. When a Cu seed layer is greater than 1000 A thickness, these contacts don't pose a serious problem. However, as the industry moves to thinner and thinner seed layers, these contacts do enough damage to cause large variations in plated film thickness. Having the actual contact point located at the end of a "moment arm" induces a certain, be it slight, amount of motion in the "x" direction in order to accommodate for the "z" motion required for sealing the wafer in the clamshell for electroplating. When the movement in the "x" direction occurs, it scratches across the seed layer reducing the number of good electrical connections.

Detailed Description Text - DETX (8):

The present inventors believe that known contact arrangements cause slight imperfections on the copper (Cu) seed layer during plating. These known contact arrangements have contact points located at the ends of, eg, 128 short "arms." These arms take up compression when, eg, sealing the wafer in a "clamshell" for electroplating. See, for example, known electroplating tools such as the SABRE Electro-fill System marketed by Novellus Systems, Inc, San Jose, Calif. See, also, previously incorporated U.S. Pat. Nos. 6,074,544 and 6,139,712. When the Cu seed layer is greater than 1000 A thickness, this doesn't pose a problem. However, as the industry moves to thinner and thinner seed layers, these contacts do enough damage to cause large variations in plated film thickness. Having the actual contact point located at the end of a "moment arm" induces a certain, be it slight, amount of motion in the "x" direction in order to accommodate for the "z" motion required for sealing the wafer in the clamshell for electroplating. When the movement in the "x" direction occurs, it scratches across the seed layer reducing the number of good electrical connections.

Detailed Description Text - DETX (11):

FIG. 3 is a diagrammatical view of an electroplating apparatus 30 having a wafer 36 mounted therein, and a vertically movable contact carrier C with fixed electrical contacts (eg, contact pins) in accordance with the present

US 6,627,052 B2

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Alternatively, a single contact (eg, an electrically conductive elastomer) could continuously engage a substrate about its perimeter. According to the present invention, a plurality of contacts could be arranged around the substrate. The plurality of contacts could all be separate structures. Such contacts may considered to be discontinuous.

As can be seen in FIG. 5B, press fitted pin contacts according to the present invention can provide electrical contact to a substrate without damaging any of the upper surface of the substrate where material is to be electrodeposited.

The shape of a contact according to the present invention may vary, depending upon the embodiment, but must make either single point contact (eg, pin 11, 11A) or continuous contact (eg, conductive elastomer). FIGS. 6, 7A and 7B illustrate various examples of embodiments of contacts according to the present invention. In the case of the straight pins or "unbuckled beam," (FIG. 7A), they could be backed with corrosion resistant conductive rubber to take up the compression of the clamshell and to tie all 128 pins to a common connection. In the case of the "buckled beam", (FIG. 7B), all pins should be wired together (shorted) before effecting the connection to the negative output lead of the DC power supply 65.

The embodiment illustrated as FIG. 4 makes contact at single points where the contacts touch the seed layer. On the other hand, the conductive elastomer CE embodiment illustrated in FIG. 5C may make contact all along its length with the seed layer and the substrate. The conductive elastomer CE having conductive filler 11E is, eg, a CHO-SEAL conductive elastomer marketed by Chromerics, Inc., Woburn, Mass.

In addition to varying the number, arrangement, and shape of the contacts, the structure of the contacts may also vary. Along these lines, the composition of the contacts may vary. According to some embodiments, the contacts may be made of copper. According to other embodiments, the contacts may be made of stainless steel. The contact or contacts may also be made of other materials. Along these lines, the contact(s) may also include a mixture of copper and beryllium.

Additionally, portions of the contacts may be made of other materials. For example, the entire contact or just a portion of the contact that contacts the substrate and/or seed layer may be coated with another material. For example, the contact or portion of the contacts that engage the seed layer and/or substrate may have a coating of α-Ta, nitrides of tantalum, gold, rhodium, and/or titanium nitride with Ti overlay, in other words, TiN/Ti. Examples of nitrides of tantalum include hexagonal-TaN and cubic-TaN.

Regardless of the composition of the contacts, they may be coated with another material. For example, the contacts may be coated with an elastomeric coating, such as VITON, or polymers, such as PTFE or PVDF (polyvinylidene fluoride) and their like. The U polymer coating may be deposited on the contacts in order to prevent wasteful metal deposition in this region.

Whether a contact is made of copper, stainless steel, or any other electrically conductive material(s), such contacts could be coated with α-Ta, nitrides of tantalum, gold, rhodium, and/or titanium nitride with Ti overlay, an elastomeric or non-elastomeric polymer coating, and/or any other material.

The backside of the substrate, that side of the substrate that does not include the seed layer, may be sealed by a seal (not shown). The seal could also be an O-ring type of seal.

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The seal, wafer, and spring may be clamped into position by a clamp. The seal may be utilized to help prevent electrolytes from coming into contact with the backside of the substrate.

The present invention includes a plating apparatus. A plating apparatus according to the present invention includes at least one contact such as those described above. FIG. 3 illustrates an embodiment of a plating apparatus according to the present invention including one embodiment of contacts according to the present invention.

The present invention also includes a method for depositing material on a surface of a substrate. The method includes engaging the substrate on which material is to be deposited with at least one contact movable only in the vertical direction. The at least one contact vertically contacts the substrate and provides an electrical connection to the substrate without obscuring the surface of the substrate to be plated. A voltage source may be connected to the at least one contact. The contacts and plating apparatus may be provided substantially as described above. The at least one contact may be biased into contact with the substrate.

As stated above, the material being deposited may be deposited over the entire surface of the substrate that it is desired the material be deposited. This is at least in part due to the fact that the contacts according to the present invention obscure the surface of the substrate on which material is being deposited. The at least one contact may be retracted. A corner of the substrate may also be engaged by the at least one contact. Also, the contact may be used to electroetch or electropolish metals on a substrate. In this case, the contacts are rendered anodic.

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention, but as aforementioned, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings, and/or the skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.

What is claimed is:

1. An apparatus for depositing material on a surface of a substrate, comprising:

at least one electrical contact movable only in a vertical direction for engagement with said surface of said substrate, and

a voltage source connected to said at least one electrical contact, wherein said at least one electrical contact is a buckled beam contact.

2. An apparatus for depositing material on a surface of a substrate, comprising:

at least one electrical contact movable only in a vertical direction for engagement with the surface of said substrate, and

a voltage source connected to said at least one electrical contact, wherein said at least one electrical contact comprises an electrically conductive elastomer.

3. An apparatus for depositing material on a surface of a substrate, comprising:

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| 1 | US 6159354 A | 20 | | | | | | | | USPAT |

US-PAT-NO: 6159354

DOCUMENT-IDENTIFIER: US 6159354 A

TITLE: Electric potential shaping method for electroplating

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US Patent No. - PN (1):
6159354

# United States Patent [19]

Contolini et al.

[11] Patent Number: 6,159,354

[45] Date of Patent: Dec. 12, 2000

[54] ELECTRIC POTENTIAL SHAPING METHOD FOR ELECTROPLATING

[75] Inventors: Robert J. Contolini, Lake Oswego; Jonathan Reid, Sherwood; Evan Patton, Portland; Jingbin Feng, Tigard; Steve Taatjes, West Linn, all of Oreg.; John Owen Dukovic, Pleasantville, N.Y.

[73] Assignees: Novellus Systems, Inc., San Jose, Calif.; International Business Machines, Inc., New York, N.Y.

[21] Appl. No.: 08/970,120

[22] Filed: Nov. 13, 1997

[51] Int. Cl.[7] ........ C25D 5/00; C25D 7/04; C25D 3/38; C25D 5/20

[52] U.S. Cl. ........ 205/96; 205/137; 205/151; 205/291; 205/148

[58] Field of Search ........ 205/151, 291, 205/96, 148; 204/DIG. 7, 137

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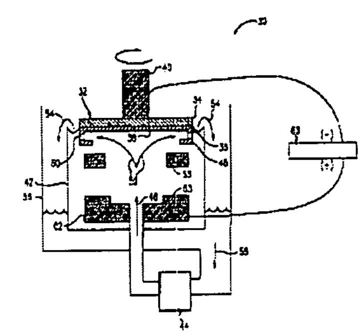
Tektronix Invention Disclosure Form (Company Confidential), not dated, 4 pages.

*Primary Examiner*—Donald R. Valentine
*Attorney, Agent, or Firm*—Skjerven, Morrill, MacPherson, Franklin and Friel

[57] ABSTRACT

An apparatus for depositing an electrically conductive layer on the surface of a wafer comprises a flange. The flange has a cylindrical wall and an annulus attached to a first end of the cylindrical wall. The annulus shields the edge region of the wafer surface during electroplating reducing the thickness of the deposited electrically conductive layer on the edge region. Further, the cylindrical wall of the flange can be provided with a plurality of apertures adjacent the wafer allowing gas bubbles entrapped on the wafer surface to readily escape.

12 Claims, 12 Drawing Sheets



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| 2 | US 4923583 A | 11 | | USPAT |
| 3 | US 4695359 A | 16 | | USPAT |

US-PAT-NO: 4923583

DOCUMENT-IDENTIFIER: US 4923583 A

TITLE: Electrode elements for filter press membrane electrolytic cells

---------- KWIC ---------

Detailed Description Text - DETX (46):

A 0.15 square meter filter press membrane electrolytic cell employing a half anode and a half cathode was fabricated. The electrodes were formed by utilizing diffusion bonding of a mesh electrode surface to generally vertical electrical conducting elements or blades and the blades to the backplates. The electrode subunits were mounted to copper conducting plates with adhesives. The titanium anode subunit was bonded to its conducting plate using the copper-filled, single-component epoxy of Example VI, after the mating surfaces were cleaned as described in Example I. A conductive coating of the type identified in Example III that lowers the electrical resistance was applied to the reverse side of the backplate in line with the conducting blades prior to mating the conducting plate to the backplate. The cathode was formed from an electrode subunit of nickel adhesively bonded to the copper conducting plate with a two-component, low viscosity, non-conductive epoxy adhesive system combined with a conducting coating that lowers the electrical resistance between the subunit backplate and the copper conducting plate. The conductive coating was applied as with the anode. The mating of the surfaces of the backplates and the copper conducting plates also employed a pressure contact joint that is a silver plated berylium copper sold commercially under the ELECTROMATE tradename.

Current US Original Classification - CCOR (1):
204/284

Current US Cross Reference Classification - CCXR (1):
204/279

Current US Cross Reference Classification - CCXR (2):
204/280

Current US Cross Reference Classification - CCXR (3):
204/288.2

Current US Cross Reference Classification - CCXR (4):
204/290.1

Current US Cross Reference Classification - CCXR (5):
204/290.12

Woodard, Jr. et al. [45] Date of Patent: May 8, 1990

[54] ELECTRODE ELEMENTS FOR FILTER PRESS MEMBRANE ELECTROLYTIC CELLS

[75] Inventors: Kenneth E. Woodard, Jr., Cleveland, Tenn.; Julius C. Fister, Jr., Hamden, Conn.; David L. Fair, Cheshire, Conn.; Robert A. Dean, Guilford, Conn.

[73] Assignee: Olin Corporation, Cheshire, Conn.

[21] Appl. No.: 795,013

[22] Filed: Nov. 4, 1985

[51] Int. Cl.⁵ ........ C25B 11/02
[52] U.S. Cl. ........ 204/286; 204/279; 204/280; 204/290 R; 204/291; 204/292; 204/293; 204/290 F; 228/193; 228/194; 228/195

[58] Field of Search ........ 204/252-254, 204/267, 268, 279, 286, 290 R, 290 F, 280, 291, 292; 228/193-195

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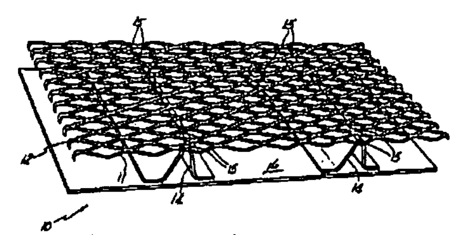
Article entitled, "Conductive Adhesives, Inks and Coatings", by Dr. Justin C. Bolger, Robert J. Astile and Silvio L. Morano.


Primary Examiner—John F. Niebling
Assistant Examiner—Kathryn Gorgos
Attorney, Agent, or Firm—Ralph D'Alessandro

[57] ABSTRACT

An electrode is provided which is formed by the metallurgical bonding technique of diffusion bonding the backplate, conductor elements and electrode surface together, then applying the catalytic coating to the electrode surface, and bonding the backplate to an electrical conducting plate.

33 Claims, 2 Drawing Sheets



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US-PAT-NO: 4749967

DOCUMENT-IDENTIFIER: US 4749967 A
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TITLE: High frequency electrical switch

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Detailed Description Text - DETX (21):
The center contact 64 is a cylindrical rod having a length of 0.445 plus or minus 0.003 inch with a diameter of 0.0254 inch corresponding to number 22 wire. The tolerance on the diameter is between plus or minus 0.015 inch inclusive and preferably closer. The center probe 40, right side probe 42, left side probe 44, and center contact 64 are all made of berylium copper alloy. When assembled, the contact sections 86, 88 of the right and left side probes 42, 44 overlap each other by approximately 0.040 inch in the vicinity of the switch contact region 100 with a tolerance which is preferably between plus or minus 0.015 in inclusive. If the overlap is too small, the center contact 64 may fail to make proper contact with one of the side probes 42, 44. On the other hand, if the overlap between the two side probes 42, 44 becomes greater than necessary to assure proper contact, the cross talk produced by switch 10 becomes unnecessarily large.

United States Patent [19]
Hoffman et al.

[11] Patent Number: 4,749,967
[45] Date of Patent: Jun. 7, 1988

[54] HIGH FREQUENCY ELECTRICAL SWITCH

[75] Inventors: Jerry Hoffman, Marina del Rey; George J. Maculewicz; Robert A. Sasak, both of Los Angeles, all of Calif.

[73] Assignee: F L Jennings Division of F L Industries, Inc., San Jose, Calif.

[21] Appl. No.: 868,282

[22] Filed: May 28, 1986

[51] Int. Cl.⁴ ........ H01P 1/10
[52] U.S. Cl. ........ 333/105; 200/153 S
[58] Field of Search ........ 333/102, 101, 105, 262; 335/4, 5; 200/153 S, 16 R, 16 C

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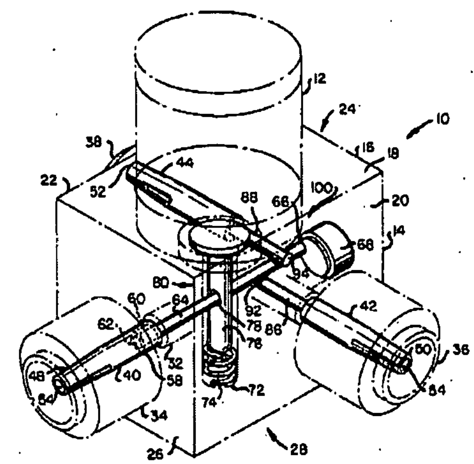
Primary Examiner—Gene Wan
Assistant Examiner—Seung Ham
Attorney, Agent, or Firm—Bogucki, Scherlacher, Mok & Roth

[57] ABSTRACT

A low cost, vibration resistant high frequency switch includes a conductive housing having bores for receiving a center probe, first and second cantilevered side probes, a floating center contact and a dielectric control rod. The center probe includes an axial bore in one end which loosely receives a first end of the low mass, wire shaped axially extending center contact. Adjacent the opposite, second end of the center contact, free ends of the side probe are spaced in a longitudinal direction perpendicular to the axial direction and extend from opposite directions into overlapping relationship with the floating center probe positioned therebetween. A solenoid controls the dielectric control rod which engages the center contact approximately midway along its length to selectively force the second end into engagement with the first or second side contact while maintaining engagement between the first end of the center contact and the center probe.

26 Claims, 7 Drawing Sheets



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| 1 | US 6551488 B1 | 45 | | | | | | | ☑ | | | | USPAT |
| 2 | US 6261433 B1 | 23 | | | | | | | ☑ | | | | USPAT |
| 3 | US 6143190 A | 46 | | | | | | ☑ | | | | | USPAT |
| 4 | US 5595637 A | 7 | | | | | | ☑ | | | | | USPAT |
| 5 | US 5334306 A | 8 | | | | | | ☑ | | | | | USPAT |
| 6 | US 4425194 A | 18 | | | | | | ☑ | | | | | USPAT |
| 7 | US 4380865 A | 9 | | | | | | ☑ | | | | | USPAT |

US-PAT-NO: 6261433

DOCUMENT-IDENTIFIER: US 6261433 B1
**See image for Certificate of Correction**

TITLE: Electro-chemical deposition system and method of electroplating on substrates

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Drawing Description Text - DRTX (8):
FIG. 4 is a schematic diagram of the electrical circuit representing the electroplating system through each contact pin and resistors.

Detailed Description Text - DETX (8):
Typically, one power supply is connected to all of the contact pins of the cathode contact member, resulting in parallel circuits through the contact pins. As the pin-to-substrate interface resistance varies, between pin locations, more current will flow, and thus more plating will occur, at the site of lowest resistance. However, by placing an external resistor in series with each contact pin, the value or quantity of electrical current passed through each contact pin becomes controlled mainly by the value of the external resistor, because the overall resistance of each contact pin-substrate contact plus the control resistor branch of the power supply to substrate circuit is substantially equal to that of the control resistor. As a result, the variations in the electrical properties between each contact pin do not affect the current distribution on the substrate, and a uniform current density results across the plating surface which contributes to uniform plating thickness. To provide a uniform current distribution between each of the contact pins 56 of the radial array configuration of cathode contact member 52, both during the plating cycle on a single substrate and between substrates in a plating run of multiple substrates, an external resistor 58 is connected in series with each contact pin 56. FIG. 4 is a schematic diagram of the electrical circuit representing the electroplating system through each contact pin of the cathode contact member 52 and the external resistor 58 connected in series with each contact pin 56. Preferably, the resistance value of the external resistor (RE.sub.EXT) 58 is greater than the resistance of any other resistive component of the circuit. As shown in FIG. 4, the electrical circuit through each contact pin 56 is represented by the resistance of each of the components connected in series with the power supply. R.sub.E represents the resistance of the electrolyte, which is typically dependent on the distance between the anode and the cathode and the composition of the electrolyte solution. R.sub.A represents the resistance of the electrolyte adjacent the substrate plating surface within the double layer and the boundary layer. R.sub.S represents the resistance of the substrate plating surface, and R.sub.C represents the resistance of the cathode contacts 56. Preferably, the resistance value of the external resistor (R.sub.EXT) is greater than the total of R.sub.E, R.sub.A, R.sub.S and R.sub.C, e.g., >1 .OMEGA. and preferably >5 .OMEGA.. The external resistor 58 also provides a uniform current distribution between different substrates of a process-sequence.

Detailed Description Text - DETX (9):
As each substrate is plated, and over multiple substrate plating cycles, the

(12) **United States Patent**
Landau

(10) Patent No.: **US 6,261,433 B1**
(45) Date of Patent: **Jul. 17, 2001**

(54) ELECTRO-CHEMICAL DEPOSITION SYSTEM AND METHOD OF ELECTROPLATING ON SUBSTRATES

(75) Inventor: Uziel Landau, Cleveland, OH (US)

(73) Assignee: Applied Materials, Inc., Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/295,678

(22) Filed: Apr. 21, 1999

Related U.S. Application Data

(60) Provisional application No. 60/082,521, filed on Apr. 21, 1998.

(51) Int. Cl.[7] ........ C25D 5/00
(52) U.S. Cl. ........ 205/96; 205/103; 205/123; 205/128; 205/149; 205/153; 205/157; 204/297.01; 204/297.03; 204/230.2; 204/230.7; 204/260; 204/261; 204/263; 204/272; 204/273; 204/275.1
(58) Field of Search ........ 204/297.01, 297.03, 204/275.1, 287, 272, 273, 260, 261, 263, 212, 213, 218, 222, 223, 228.9, 229.1, 229.2, 229.6, 230.2, 230.7; 205/96, 103, 123, 128, 149, 153, 157, 291, 292

(56) References Cited

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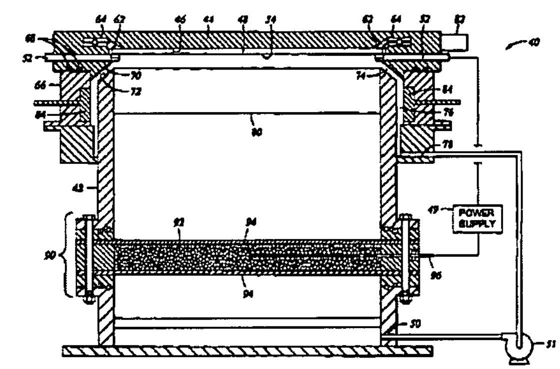
(List continued on next page.)

*Primary Examiner*—Bruce F. Bell
(74) *Attorney, Agent, or Firm*—Thomason, Moser & Patterson, L.L.P.

(57) ABSTRACT

The invention provides an apparatus and a method for achieving reliable, consistent metal electroplating or electrochemical deposition onto semiconductor substrates. More particularly, the invention provides uniform and void-free deposition of metal onto metal seeded semiconductor substrates having sub-micron, high aspect ratio features. The invention provides an electrochemical deposition cell comprising a substrate holder, a cathode electrically contacting a substrate plating surface, an electrolyte container having an electrolyte inlet, an electrolyte outlet and an opening adapted to receive a substrate plating surface and an anode electrically connect to an electrolyte. Preferably, a vibrator is attached to the substrate holder to vibrate the substrate in at least one direction, and an auxiliary electrode is disposed adjacent the electrolyte outlet to provide uniform deposition across the substrate surface. Preferably, a periodic reverse current is applied during the plating period to provide a void-free metal layer within high aspect ratio features on the substrate.

29 Claims, 7 Drawing Sheets

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| 3 | US 6143190 A | 46 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 4 | US 5595637 A | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 5 | US 5334306 A | 8 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 6 | US 4425194 A | 18 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 7 | US 4380865 A | 9 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |

Detailed Description Text - DETX (9):

As each substrate is plated, and over multiple substrate plating cycles, the contact-pin-substrate interface resistance still may vary, eventually reaching an unacceptable value. An electronic sensor/alarm 60 can be connected across the external resistor 58 to monitor the voltage/current across the external resistor to address this problem. If the voltage/current across any external resistor 58 falls outside of a preset operating range that is indicative of a high pin-substrate resistance, the sensor/alarm 60 triggers corrective measures such as shutting down the plating process until the problems are corrected by an operator. Alternatively, a separate power supply can be connected to each contact pin and can be separately controlled and monitored to provide a uniform current distribution across the substrate.

Claims Text - CLTX (19):

b) a cathode electrically contacting the substrate plating surface, wherein the cathode comprises a cathode contact member disposed at a peripheral portion of the substrate plating surface, the cathode contact member having a contact surface adapted to electrically contact the substrate surface, wherein the cathode contact member comprises a radial array of contact pins and a resistor connected in series with each contact pin;

Current US Cross Reference Classification - CCXR (12):
205/123

Current US Cross Reference Classification - CCXR (16):
205/157



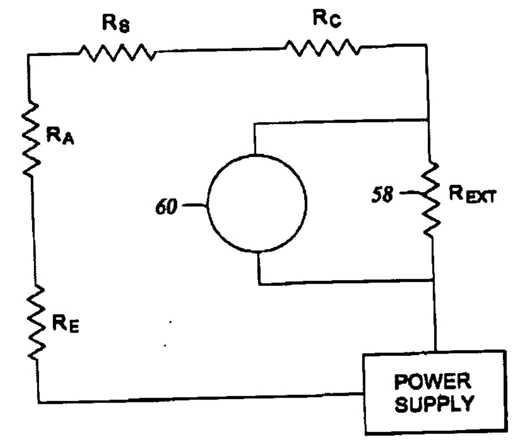


Fig. 4

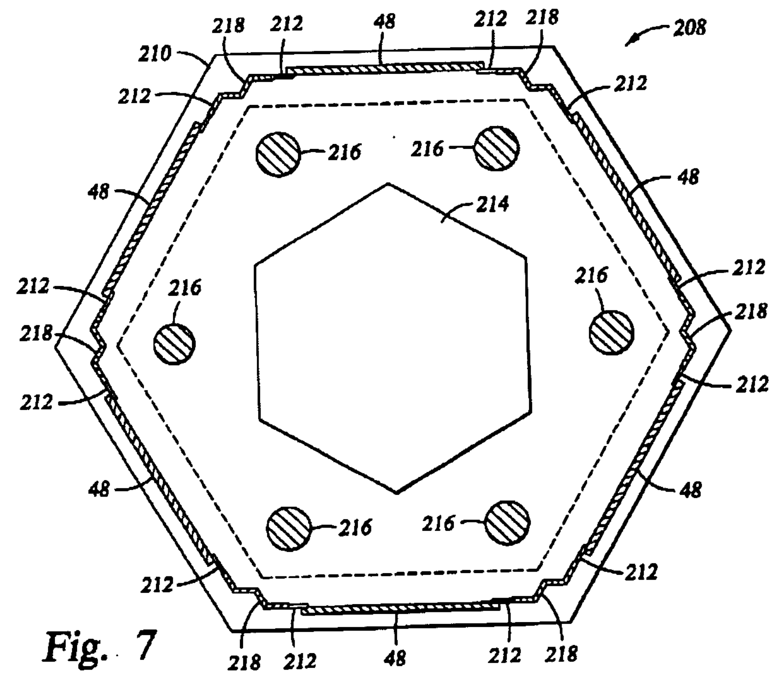


Fig. 7

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  - L2: (1486933) contact or contacts
  - L3: (21210) (thick adj film) or thick-film
  - L4: (1551) l3 near2 (resistor or resistors)
  - L6: (246) l4 same l2
  - L7: (0) l6 and l1
  - L8: (14572) (205/50-333).CCLS.
  - L9: (0) l6 and l8
  - L11: (0) l4 and l1
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| 1 | ☑ | ☐ | ☐ | ☐ | US 4288530 A | 19810908 | 6 | Method of tuning apparatus by low power laser beam | 430/315 | 205/135; 205/221; | | Bedard, Brian E. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |

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  - L1: (610) ((205/123) or (205/157)).CCLS.
  - L2: (1486933) contact or contacts
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  - L4: (1551) 13 near2 (resistor or resistors)
  - L6: (246) 14 same 12
  - L7: (0) 16 and 11
  - L8: (14572) (205/50-333).CCLS.
  - L9: (0) 16 and 18
  - L11: (0) 14 and 11
  - L12: (1) 14 and 18
  - L13: (16892) (204/198-297.16).CCLS.
  - L14: (1) 16 and 113
  - L15: (1) 14 and 114
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| 1 | ☐ | ☐ | ☐ | ☐ | US 3917524 A | 19751104 | 9 | Electrochemical cell assembly | 204/411 | 204/274; 204/278.5; | | Connery, James G. et al. | ☑ | ☐ | ☐ | ☐ | ☐ | ☐ |

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  - L1: (610) ((205/123) or (205/157)).CCLS.
  - L2: (1486933) contact or contacts
  - L3: (21210) (thick adj film) or thick-film
  - L4: (1551) l3 near2 (resistor or resistors)
  - L6: (246) l4 same l2
  - L7: (0) l6 and l1
  - L8: (14572) (205/50-333).CCLS.
  - L9: (0) l6 and l8
  - L11: (0) l4 and l1
  - L12: (1) l4 and l8
  - L13: (16892) (204/198-297.16).CCLS.
  - L14: (1) l6 and l13
  - L15: (1) l4 and l14
  - L16: (255810) resistor or resistors
  - L18: (45007) l2 same l16
  - L19: (16) l18 and l1
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| 1 | ☑ | ☐ | ☐ | ☐ | US 20030168346 A1 | 20030911 | 46 | Segmenting of processing system into wet and dry | 205/157 | | | Hey, H. Peter W. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 2 | ☑ | ☐ | ☐ | ☐ | US 20020029961 A1 | 20020314 | | Electro-chemical deposition system | 204/198 | 204/212; 204/228.1; | | Dordi, Yezdi et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 3 | ☑ | ☐ | ☐ | ☐ | US 6551488 B1 | 20030422 | | Segmenting of processing system into wet and dry | 205/157 | 204/198; 204/224M; | | Hey, H. Peter W. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 4 | ☑ | ☐ | ☐ | ☐ | US 6261433 B1 | 20010717 | | Electro-chemical deposition system and method of | 205/96 | 204/230.2; 204/230.7; | | Landau, Uziel | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 5 | ☑ | ☐ | ☐ | ☐ | US 6143190 A | 20001107 | | Method of producing a through-hole, silicon | 216/27 | 205/157; 205/171; | | Yagi, Takayuki et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 6 | ☑ | ☐ | ☐ | ☐ | US 5595637 A | 19970121 | | Photoelectrochemical fabrication of electronic | 205/91 | 205/123; 205/137; | | Tench, D. Morgan et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 7 | ☑ | ☐ | ☐ | ☐ | US 5334306 A | 19940802 | | Metallized paths on diamond surfaces | 205/131 | 205/118; 205/123; | | Dautremont-Smith, William C. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 8 | ☑ | ☐ | ☐ | ☐ | US 4425194 A | 19840110 | | Photo-voltaic power generating means and methods | 205/157 | 136/255; 136/258; | | Kroger, Ferdinand A. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 9 | ☑ | ☐ | ☐ | ☐ | US 4380865 A | 19830426 | | Method of forming dielectrically isolated | 438/409 | 205/157; 205/656; | | Frye, Robert C. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 10 | ☑ | ☐ | ☐ | ☐ | US 4293637 A | 19811006 | | Method of making metal electrode of semiconductor | 438/614 | 205/123; 205/135; | | Hatada, Kenzo et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 11 | ☑ | ☐ | ☐ | ☐ | US 4188707 A | 19800219 | | Semiconductor devices and method of manufacturing the | 438/301 | 148/DIG.124; 148/DIG.18; | | Asano, Masaru et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 12 | ☑ | ☐ | ☐ | ☐ | US 4011144 A | 19770308 | | Methods of forming metallization patterns on | 438/611 | 205/123; 257/736; | | Bachman, Albert K. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |

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  - L1: (609) ((205/123) or (205/157)).CCLS.
  - L2: (1479716) contact or contacts
  - L3: (809533) resistance
  - L4: (132389) l2 same l3
  - L5: (108) l1 and l4
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  - L1: (609) ((205/123) or (205/157)).CCLS.
  - L2: (1479716) contact or contacts
  - L3: (809533) resistance
  - L4: (132389) l2 same l3
  - L5: (108) l4 and l1
- Failed
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| 12 | US 6448644 B1 | 15 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 13 | US 6440291 B1 | 10 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 14 | US 6440289 B1 | 9 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 15 | US 6426290 B1 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 16 | US 6413404 B1 | 13 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 17 | US 6409903 B1 | 8 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 18 | US 6402923 B1 | 11 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6402923

DOCUMENT-IDENTIFIER: US 6402923 B1
**See image for Certificate of Correction**

TITLE: Method and apparatus for uniform electroplating of integrated circuits using a variable field shaping element

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Brief Summary Text - BSTX (10):
The seed layer initially has a significant resistance radially from the edge to the center of the wafer because the seed layer is initially very thin. This resistance causes a corresponding potential drop from the edge where electrical contact is made to the center of the wafer. These effects are reported in L. A. Gochberg, "Modeling of Uniformity and 300-mm Scale-up in a Copper Electroplating Tool", Proceedings of the Electrochemical Society (Fall 1999, Honolulu Hawaii); and E. R. Broadbent, E. J. McInerney, L. C. Gochberg, and R. L. Jackson, "Experimental and Analytical Study of Seed Layer Resistance for Copper Damascene Electroplating", Vac. Sci. & Technol. B17, 2584 (November/December 1999). Thus, the seed layer has a nonuniform initial potential that is more negative at the edge of the wafer. The associated deposition rate tends to be greater at the wafer edge relative to the interior of the wafer. This effect is known as the `terminal effect.`

Brief Summary Text - BSTX (19):
Regarding the trend towards larger diameter wafers, it is generally understood that the deposition rate, as measured by layer thickness, can be maintained by scaling total current through the electrochemical reactor in proportion to the increased surface area of the larger wafer. Thus, a 300 mm wafer requires 2.25 times more current than does a 200 mm wafer. Electroplating operations are normally performed by using a clamshell wafer holder that contacts the wafer only at its outer radius. Due to this mechanical arrangement, the total resistance from the edge of the wafer to the center of the wafer is independent of the radius. Nevertheless, with the higher applied current at the edge of the larger wafer, which is required to maintain the same current density for process uniformity, the total potential drop from the edge to the center of the wafer is greater for the larger diameter wafer. This circumstance leads to an increased rate of deposition (layer thickness) with radius. While the problem of increasing deposition rate with radius exists for all wafers, it is exacerbated in the case of larger wafers. At sufficiently large wafer sizes, the difference in current density at the center versus the edge will lead to incomplete fill at one of those locations.

Current US Cross Reference Classification - CCXR (5):
205/123

Current US Cross Reference Classification - CCXR (6):
205/157

(12) **United States Patent**
Mayer et al.

(10) Patent No.: **US 6,402,923 B1**
(45) Date of Patent: **Jun. 11, 2002**

(54) **METHOD AND APPARATUS FOR UNIFORM ELECTROPLATING OF INTEGRATED CIRCUITS USING A VARIABLE FIELD SHAPING ELEMENT**

(76) Inventors: **Steven T. Mayer**, 17867 Sundown Ct., Lake Oswego, OR (US) 97034; **Richard Hill**, 187 Heather Dr., San Jose, CA (US) 94027; **Alain Harrus**, 517 Patricia La., Palo Alto, CA (US) 94303; **Evan Patton**, 2972 SW. Collins Ct., Portland, OR (US) 97219; **Robert Contolini**, 5575 Suncreek Dr., Lake Oswego, OR (US) 97035; **Steve Taatjes**, 1331 High Touch St., West Linn, OR (US) 97068; **Jon Reid**, 420 SW. Madrona La., Sherwood, OR (US) 97140

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/537,467
(22) Filed: Mar. 27, 2000
(51) Int. Cl.7 ........ C25D 5/00
(52) U.S. Cl. ........ 205/96; 204/224 R; 204/297.05; 204/DIG. 7; 204/118; 204/123; 204/157
(58) Field of Search ........ 204/224 R, 297.05, 204/DIG. 7, 229.8; 205/122, 123, 125, 96, 97, 118, 157

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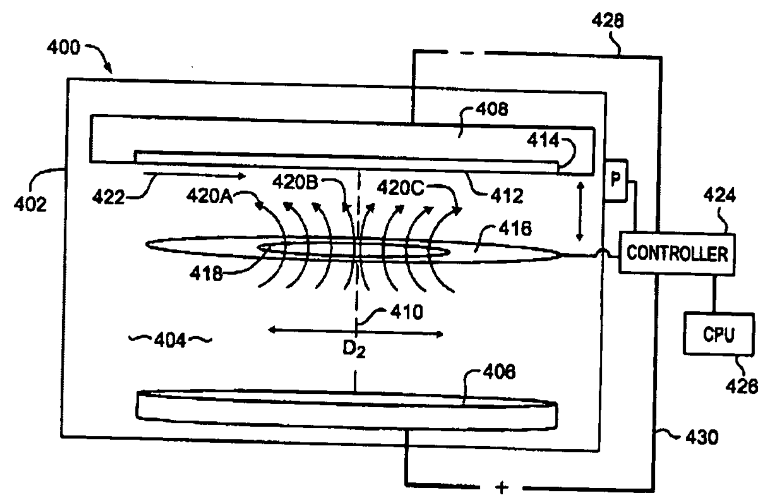
*Primary Examiner*—Donald R. Valentine
*Assistant Examiner*—Wesley A. Nicolas
(74) *Attorney, Agent, or Firm*—Thomas Swenson; Lathrop & Gage, L.C.

(57) ABSTRACT

An electrochemical reactor is used to electrofill damascene architecture for integrated circuits. A shield is used to screen the applied field during electroplating operations to compensate for potential drop along the radius of a wafer. The shield establishes an inverse potential drop in the electrolytic fluid to overcome the resistance of a thin film seed layer of copper on the wafer.

25 Claims, 4 Drawing Sheets

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| 14 | US 6440289 B1 | 9 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
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| 20 | US 6299751 B1 | 45 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6299751

DOCUMENT-IDENTIFIER: US 6299751 B1

TITLE: Apparatus and method for plating wafers, substrates and other articles

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Brief Summary Text - BSTX (15):

A seventh aspect of the invention is an apparatus and method for plating a wafer that is particularly useful in improving the uniformity of the plating deposition across the surface of the wafer when the wafer is initially being plated. When the wafer is initially being plated, the surface resistance of the wafer is high due to the high resistive properties of the seed layer (e.g. copper seed layer). As a result, more of the plating is deposited where the cathode makes contact to the wafer (e.g. at the perimeter of the wafer). This aspect of the invention comprises providing a secondary cathode situated near the cathode contact of the wafer to reduce the plating rate near the cathode contact in response to a control voltage that is more negative than the cathode. The more negative voltage on the secondary cathode diverts plating ions that would otherwise be deposited near the cathode contact. The control voltage is selected to improve the uniformity of the plating deposition across the surface of the wafer.

Detailed Description Text - DETX (22):

In the preferred embodiment, the cathode contact comprises an electrical-conductive fluid, such as a mixture of sulfuric acid and de-ionized (DI) water. The conductive fluid is significantly advantageous because it provides a uniform contact along and within the exclusion zone (i.e. the contact has a uniform resistance along and within the exclusion zone). Because of the continuity of the cathode contact provided by the conductive fluid, a more uniform plating deposition and higher currents for increasing the plating rate results. Alternatively, a mechanical contact comprising a plurality of equally spaced contacts can be provided along and within the exclusion zone to effectuate the cathode contact to the wafer.

Detailed Description Text - DETX (64):

The advantage of using a conductive fluid versus a mechanical contact in making the cathode connection to the wafer 308 is that the fluid contact does not typically damage the wafer, whereas a mechanical contact tends to warp and/or deform the wafer. Another advantage of the fluid contact is that it provides a relatively large contact surface area since the contact is continuous throughout the "cathode contact area." For example, the two (2) millimeter wide cathode contact area amounts to approximately a two (2) square-inch surface area. That is substantial considering how small the width of the "cathode contact area" is. Because of the relatively large contact surface area, the resistance of the contact is relatively small. This increases the current carrying capacity of the contact, which can lead to much higher plating rates. Yet another advantage of the conductive fluid contact is that the electrical contact is more uniform throughout the "cathode contact area." This results is a more uniform plating deposition across the surface of the wafer. Still another advantage of the conductive fluid, particularly if it

(12) **United States Patent**
Kaufman et al.

(10) Patent No.: **US 6,299,751 B1**
(45) Date of Patent: **Oct. 9, 2001**

(54) **APPARATUS AND METHOD FOR PLATING WAFERS, SUBSTRATES AND OTHER ARTICLES**

(75) Inventors: Robert Kaufman, Canoga Park; Gary C. Downes, Moorpark, both of CA (US)

(73) Assignee: Technic Inc., Cranston, RI (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/638,982

(22) Filed: Aug. 15, 2000

Related U.S. Application Data

(62) Division of application No. 09/348,768, filed on Jul. 7, 1999, now Pat. No. 6,197,182.

(51) Int. Cl.$^7$ ........ C25D 5/20; C25D 21/10; C25D 7/00; C25D 5/08

(52) U.S. Cl. ........ 205/148; 205/149; 205/157; 205/133

(58) Field of Search ........ 427/430.1; 438/584, 438/678, 679, 680; 205/148, 149, 157, 133

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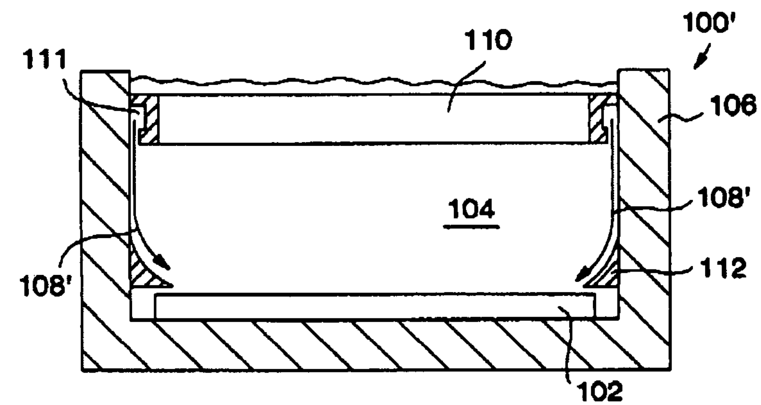
* cited by examiner

Primary Examiner—Edna Wong
(74) Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman LLP

(57) ABSTRACT

A plating apparatus and methodology is disclosed that is particularly useful in improving the plating rate, improving the plating of via holes, improving the uniformity of the plating deposition across the surface of the wafer, and minimizing damage to the wafer. With regard to improving the plating rate and the plating of via holes, the plating apparatus and method immerses a wafer in a plating fluid bath and continuously directs plating fluid towards the surface of the wafer. Immersing the wafer in a plating fluid bath reduces the occurrence of trapped gas pockets within via holes which makes it easier to plate them. The continuous directing of plating fluid towards the surface of the wafer increases the ion concentration gradient which is, in turn, increases the plating rate. With regard to improving the uniformity of the plating deposition, the plating apparatus and method effectuate random horizontal fluid flow within the bath to reduce the occurrence of relatively long horizontal fluid flow that causes non-uniform plating deposition across the surface of the wafer.

16 Claims, 27 Drawing Sheets

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| 27 | US 6274023 B1 | 45 | USPAT |
| 28 | US 6267862 B1 | 45 | USPAT |
| 29 | US 6261433 B1 | 23 | USPAT |

Detailed Description Text - DETX (8):

Typically, one power supply is connected to all of the contact pins of the cathode contact member, resulting in parallel circuits through the contact pins. As the pin-to-substrate interface resistance varies, between pin locations, more current will flow, and thus more plating will occur, at the site of lowest resistance. However, by placing an external resistor in series with each contact pin, the value or quantity of electrical current passed through each contact pin becomes controlled mainly by the value of the external resistor, because the overall resistance of each contact pin-substrate contact plus the control resistor branch of the power supply to substrate circuit is substantially equal to that of the control resistor. As a result, the variations in the electrical properties between each contact pin do not affect the current distribution on the substrate, and a uniform current density results across the plating surface which contributes to uniform plating thickness. To provide a uniform current distribution between each of the contact pins 56 of the radial array configuration of cathode contact member 52, both during the plating cycle on a single substrate and between substrates in a plating run of multiple substrates, an external resistor 58 is connected in series with each contact pin 56. FIG. 4 is a schematic diagram of the electrical circuit representing the electroplating system through each contact pin of the cathode contact member 52 and the external resistor 58 connected in series with each contact pin 56. Preferably, the resistance value of the external resistor (RE.sub.EXT) 58 is greater than the resistance of any other resistive component of the circuit. As shown in FIG. 4, the electrical circuit through each contact pin 56 is represented by the resistance of each of the components connected in series with the power supply. R.sub.E represents the resistance of the electrolyte, which is typically dependent on the distance between the anode and the cathode and the composition of the electrolyte solution. R.sub.A represents the resistance of the electrolyte adjacent the substrate plating surface within the double layer and the boundary layer. R.sub.S represents the resistance of the substrate plating surface, and R.sub.C represents the resistance of the cathode contacts 56. Preferably, the resistance value of the external resistor (R.sub.EXT) is greater than the total of R.sub.E, R.sub.A, R.sub.S and R.sub.C, e.g., >1 .OMEGA. and preferably >5 .OMEGA.. The external resistor 58 also provides a uniform current distribution between different substrates of a process-sequence.

Detailed Description Text - DETX (9):

As each substrate is plated, and over multiple substrate plating cycles, the contact-pin-substrate interface resistance still may vary, eventually reaching an unacceptable value. An electronic sensor/alarm 60 can be connected across the external resistor 58 to monitor the voltage/current across the external resistor to address this problem. If the voltage/current across any external resistor 58 falls outside of a preset operating range that is indicative of a high pin-substrate resistance, the sensor/alarm 60 triggers corrective measures such as shutting down the plating process until the problems are corrected by an operator. Alternatively, a separate power supply can be connected to each contact pin and can be separately controlled and monitored to provide a uniform current distribution across the substrate.

Current US Cross Reference Classification - CCXR (12):
205/123

Current US Cross Reference Classification - CCXR (16):
205/157

US 6,261,433 B1

1

# ELECTRO-CHEMICAL DEPOSITION SYSTEM AND METHOD OF ELECTROPLATING ON SUBSTRATES

## CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application Ser. No. 60/082,521, entitled "Electroplating on Substrates," filed on Apr. 21, 1998.

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to deposition of a metal layer onto a substrate. More particularly, the present invention relates to an apparatus and a method for electroplating a metal layer onto a substrate.

2. Background of the Related Art

Sub-micron multi-level metallization is one of the key technologies for the next generation of ultra large scale integration (ULSI). The multilevel interconnects that lie at the heart of this technology require planarization of interconnect features formed in high aspect ratio apertures, including contacts, vias, lines and other features. Reliable formation of these interconnect features is very important to the success of ULSI and to the continued effort to increase circuit density and quality on individual substrates and die.

As circuit densities increase, the widths of vias, contacts and other features, as well as the dielectric materials between them, decrease to sub-micron dimensions, whereas the thickness of the dielectric layers remains substantially constant, with the result that the aspect ratios for the features, i.e., their height divided by width, increases. Many traditional deposition processes have difficulty filling sub-micron structures where the aspect ratio exceed 2:1, and particularly where it exceeds 4:1. Therefore, there is a great amount of ongoing effort being directed at the formation of void-free, sub-micron features having high aspect ratios.

Elemental aluminum (Al) and its alloys have been the traditional metals used to form lines and plugs in semiconductor processing because of aluminum's low electrical resistivity, its superior adhesion to silicon dioxide ($SiO_2$), its ease of patterning, and the ability to obtain it in a highly pure form. However, aluminum has a higher electrical resistivity than other more conductive metals such as copper and silver, and aluminum also can suffer from electromigration phenomena. Electromigration is considered as the motion of atoms of a metal conductor in response to the passage of high current density through it, and it is a phenomenon that occurs in a metal circuit while the circuit is in operation, as opposed to a failure occurring during fabrication. Electromigration can lead to the formation of voids in the conductor. A void may accumulate and/or grow to a size where the immediate cross-section of the conductor is insufficient to support the quantity of current passing through the conductor, and may also lead to an open circuit. The area of conductor available to conduct heat therealong likewise decreases where the void forms, increasing the risk of conductor failure. This problem is sometimes overcome by doping aluminum with copper and with tight texture or crystalline structure control of the material. However, electromigration in aluminum becomes increasingly problematic as the current density increases.

Copper and its alloys have lower resistivity than aluminum and higher electromigration resistance as compared to aluminum. These characteristics are important for supporting the higher current densities experienced at high levels of integration and increased device speed. Copper also has good thermal conductivity and is available in a highly pure state. Therefore, copper is becoming a choice metal for filling sub-micron, high aspect ratio interconnect features on semiconductor substrates.

2

Despite the desirability of using copper for semiconductor device fabrication, choices of fabrication methods for depositing copper into high aspect ratio features are limited. Precursors for CVD deposition of copper are ill-developed and involve complex and costly chemistry. Physical vapor deposition into such features produces unsatisfactory results because of limitations in 'step coverage' and voids formed in the features.

As a result of these process limitations, electroplating, which had previously been limited to the fabrication of patterns on circuit boards, is just now emerging as a method to fill vias and contacts on semiconductor devices. FIGS. 1A–1E illustrate a metallization technique for forming a dual damascene interconnect in a dielectric layer having dual damascene via and wire definitions, wherein the via has a floor exposing an underlying layer. Although a dual damascene structure is illustrated, this method can be applied also to metallize other interconnect features. The method generally comprises physical vapor depositing a barrier layer over the feature surfaces, physical vapor depositing a conductive metal seed layer, preferably copper, over the barrier layer, and then electroplating a conductive metal over the seed layer to fill the structure/feature. Finally, the deposited layers and the dielectric layers are planarized, such as by chemical mechanical polishing (CMP), to define a conductive interconnect feature.

Referring to FIGS. 1A through 1E, a cross sectional diagram of a layered structure 10 is shown including a dielectric layer 16 formed over an underlying layer 14 which contains electrically conducting features 15. The underlying layer 14 may take the form of a doped silicon substrate or it may be a first or subsequent conducting layer formed on a substrate. The dielectric layer 16 is formed over the underlying layer 14 in accordance with procedures known in the art such as dielectric CVD to form a part of the overall integrated circuit. Once deposited, the dielectric layer 16 is patterned and etched to form a dual damascene via and wire definition, wherein the via has a floor 30 exposing a small portion of the conducting feature 15. Etching of the dielectric layer 16 can be accomplished with various generally known dielectric etching processes, including plasma etching.

Referring to FIG. 1A, a cross-sectional diagram of a dual damascene via and wire definition formed in the dielectric layer 16 is shown. The via and wire definition facilitates the deposition of a conductive interconnect that will provide an electrical connection with the underlying conductive feature 15. The definition provides vias 32 having via walls 34 and a floor 30 exposing at least a portion of the conductive feature 15, and trenches 17 having trench walls 38.

Referring to FIG. 1B, a barrier layer 20 of tantalum or tantalum nitride (TaN) is deposited on the via and wire definition, such that aperture 18 remains in the via 32, by using reactive physical vapor deposition, i.e., by sputtering a tantalum target in a nitrogen/argon plasma. Preferably, where the aspect ratio of the aperture is high (e.g. 4:1 or higher) with a sub-micron wide via, the Ta/TaN is deposited in a high density plasma environment, wherein the sputtered deposition of the Ta/TaN is ionized and drawn perpendicularly to the substrate by a negative bias on the substrate. The

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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | US 6607650 B1 | 20 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 2 | US 6576113 B1 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 3 | US 6565729 B2 | 53 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 4 | US 6562715 B1 | 16 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 5 | US 6551488 B1 | 44 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 6 | US 6540899 B2 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 7 | US 6497805 B2 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6540899

DOCUMENT-IDENTIFIER: US 6540899 B2

TITLE: Method of and apparatus for fluid sealing, while electrically contacting, wet-processed workpieces

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Brief Summary Text - BSTX (5):

Making a reliable and uniform electrical contact to the edge of a workpiece and, at the same time sealing the edge against fluid invasion is a recognized and difficult problem in the art of high precision electrodeposition on workpieces such as semiconductor wafers and the like. During such electrodeposition, if the electrical contact to the workpiece is not uniform or if the contact has high resistance to current flow, the desired uniform deposited film may not be achieved. A variety of means for trying to solve this problem have accordingly been proposed in the prior art over the years and will now be briefly summarized.

Brief Summary Text - BSTX (19):

To achieve these objectives, the invention includes a plurality of narrow flexible fingers that form an assembly and are embedded in the elastomeric material; for example, 360 fingers may be used to seal and contact the perimeter of a 200 millimenter wafer. For applications where electrical contact to the workpiece is required, a small region of each flexible finger, the contact tip surface, may be exposed through the surface of the elastomer, with this small contact region preferably coated with a film of gold, platinum, palladium, or other low-resistence electrical contact metal. A sealing bead is defined in said elastomer during the molding over the flexible finger assembly, with such sealing bead positioned adjacent to the contact region, toward the workpiece center--preferably, in practice, less than 0.021" away from the contact region, as later more fully explained. In a typical application of the invention, force is applied between the backside of the workpiece and the flexible finger assembly so that the elastomeric sealing bead is compressed against the workpiece surface to create a temporary fluid seal, and the flexible contact tips are pressed against the workpiece surface to create a plurality of low resistance electrical contacts that form a virtually continuous path of current entry around the workpiece perimeter region. In particular, as the flexible fingers deform, they each slide a small amount radially along the workpiece surface which serves beneficially to break up any oxides or contamination on the workpiece surface and enables a very low contact resistance temporary connection to be achieved between the flexible fingers and the workpiece surface.

Detailed Description Text - DETX (9):

The before-mentioned recess 29 in the molded encasement adjacent to the contact surface 26 insures that, as the flexure finger 36 deflects at 62, the workpiece edge 23 does not contact the sealing element 14 and does not lift the workpiece 20 off of the metal contact surface 26. This rotational deflection 62 may be considered to have a horizontal component 64 and a vertical component 66. Of particular advantage for the purpose of making electrical contact to the workpiece 20 is the horizontal component of motion 64. Though this motion

U.S. Patent Apr. 1, 2003 Sheet 3 of 6 US 6,540,899 B2

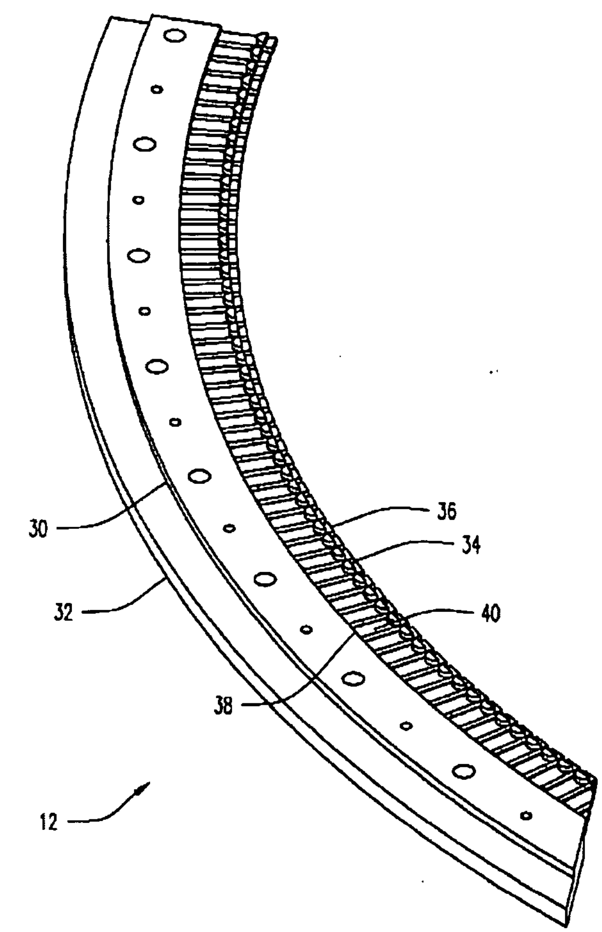


FIG. 4

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| 14 | US 6440289 B1 | 9 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 15 | US 6426290 B1 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 16 | US 6413404 B1 | 13 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 17 | US 6409903 B1 | 8 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 18 | US 6402923 B1 | 11 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 19 | US 6344126 B1 | 6 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 20 | US 6299751 B1 | 45 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6299751

DOCUMENT-IDENTIFIER: US 6299751 B1

TITLE: Apparatus and method for plating wafers, substrates and other articles

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Brief Summary Text - BSTX (15):

A seventh aspect of the invention is an apparatus and method for plating a wafer that is particularly useful in improving the uniformity of the plating deposition across the surface of the wafer when the wafer is initially being plated. When the wafer is initially being plated, the surface resistance of the wafer is high due to the high resistive properties of the seed layer (e.g. copper seed layer). As a result, more of the plating is deposited where the cathode makes contact to the wafer (e.g. at the perimeter of the wafer). This aspect of the invention comprises providing a secondary cathode situated near the cathode contact of the wafer to reduce the plating rate near the cathode contact in response to a control voltage that is more negative than the cathode. The more negative voltage on the secondary cathode diverts plating ions that would otherwise be deposited near the cathode contact. The control voltage is selected to improve the uniformity of the plating deposition across the surface of the wafer.

Detailed Description Text - DETX (22):

In the preferred embodiment, the cathode contact comprises an electrical-conductive fluid, such as a mixture of sulfuric acid and de-ionized (DI) water. The conductive fluid is significantly advantageous because it provides a uniform contact along and within the exclusion zone (i.e. the contact has a uniform resistance along and within the exclusion zone). Because of the continuity of the cathode contact provided by the conductive fluid, a more uniform plating deposition and higher currents for increasing the plating rate results. Alternatively, a mechanical contact comprising a plurality of equally spaced contacts can be provided along and within the exclusion zone to effectuate the cathode contact to the wafer.

Detailed Description Text - DETX (64):

The advantage of using a conductive fluid versus a mechanical contact in making the cathode connection to the wafer 308 is that the fluid contact does not typically damage the wafer, whereas a mechanical contact tends to warp and/or deform the wafer. Another advantage of the fluid contact is that it provides a relatively large contact surface area since the contact is continuous throughout the "cathode contact area." For example, the two (2) millimeter wide cathode contact area amounts to approximately a two (2) square-inch surface area. That is substantial considering how small the width of the "cathode contact area" is. Because of the relatively large contact surface area, the resistance of the contact is relatively small. This increases the current carrying capacity of the contact, which can lead to much higher plating rates. Yet another advantage of the conductive fluid contact is that the electrical contact is more uniform throughout the "cathode contact area." This results is a more uniform plating deposition across the surface of the wafer. Still another advantage of the conductive fluid, particularly if it

U.S. Patent Oct. 9, 2001 Sheet 14 of 27 US 6,299,751 B1

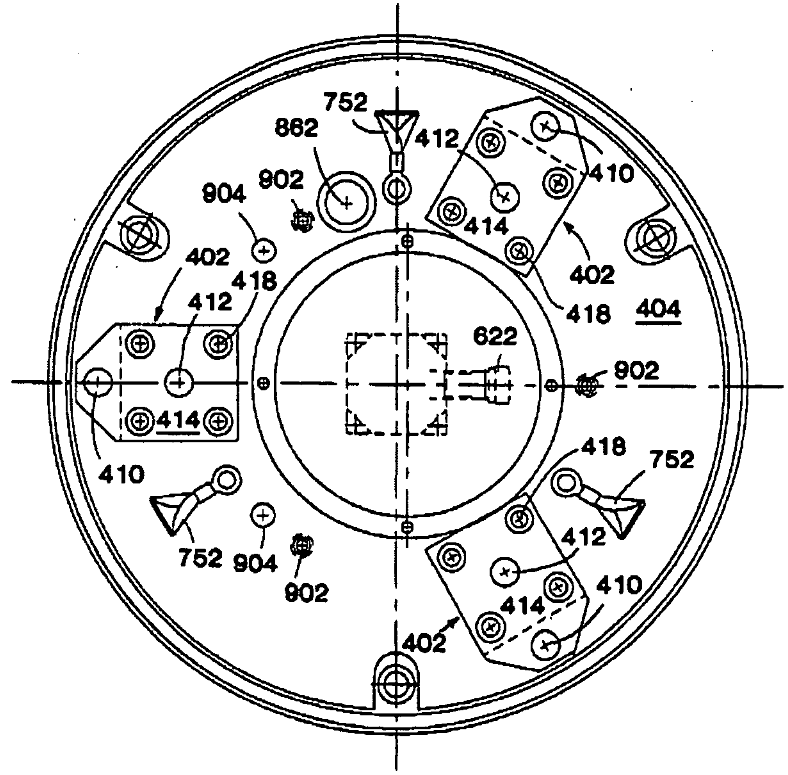


FIG. 16

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| 28 | US 6267862 B1 | 45 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 29 | US 6261433 B1 | 23 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 30 | US 6251250 B1 | 17 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 31 | US 6207034 B1 | 9 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 32 | US 6197182 B1 | 45 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 33 | US 6187165 B1 | 9 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 34 | US 6187164 B1 | 13 | ☐ | ☑ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6187164

DOCUMENT-IDENTIFIER: US 6187164 B1
**See image for Certificate of Correction**

TITLE: Method for creating and testing a combinatorial array employing individually addressable electrodes

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Brief Summary Text - BSTX (5):
Electroplating has been employed in small scale as well as industrial processes. For example, electroplating of precious metals to improve the appearance of an article or to create special effects is well known. Electroplating is also employed to improve the corrosion resistance of corrosive substances by depositing thin surface films of corrosion resistant metals such as zinc, tin, chromium, nickel and others. Wear resistant and friction modifying coatings of nickel, chromium, titanium and other metals and their alloys are used to improve the wear resistance of bearing surfaces. Electroplating is also employed in the electronics industry to improve or modify the electrical properties of substrates such as contacts, printed circuits, electrical conductors, and other electrical items in which specific surface or surface-to-substrate conductive properties are desired. Distinct metals are often electroplated onto metal surfaces to improve soldering characteristics or to facilitate subsequent coating by painting or application of other adhering films such as plastics, adhesives, rubber, or other materials.

Current US Cross Reference Classification - CCXR (3):
205/123

(12) **United States Patent**
Warren et al.

(10) Patent No.: **US 6,187,164 B1**
(45) Date of Patent: **Feb. 13, 2001**

(54) **METHOD FOR CREATING AND TESTING A COMBINATORIAL ARRAY EMPLOYING INDIVIDUALLY ADDRESSABLE ELECTRODES**

(75) Inventors: **Christopher J. Warren**, Mountain View; **Robert C. Haushalter**, Los Gatos; **Leonid Matsiev**, Cupertino, all of CA (US)

(73) Assignee: Symyx Technologies, Inc., Santa Clara, CA (US)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: 09/119,187

(22) Filed: Jul. 20, 1998

**Related U.S. Application Data**

(63) Continuation-in-part of application No. 08/941,170, filed on Sep. 30, 1997.

(51) Int. Cl.[7] ..................... C25D 5/02; C25D 21/12

(52) U.S. Cl. ..................... 205/81; 205/118; 205/122; 205/123; 205/136; 205/775; 205/782

(58) Field of Search ..................... 205/122, 118, 205/123, 228, 81, 136, 775, 782; 204/224, 230.7, 230.1

(56) **References Cited**

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Chu, Deryn, et al. *J. Electrochem. Soc.*, vol. 143, No. 5, pp. 1685–1690, (1996). Month of publication not available.

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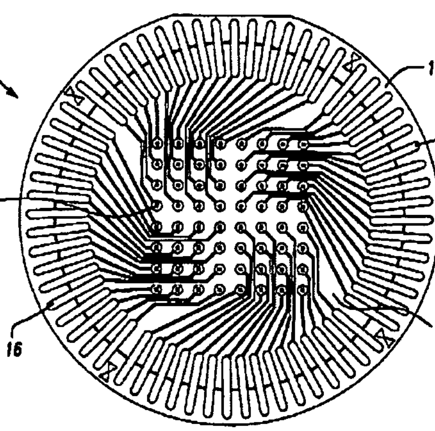
*Primary Examiner*—Kathryn Gorgos
*Assistant Examiner*—William T. Leader
(74) *Attorney, Agent, or Firm*—Dobrusin Darden; Thennisch & Lorenz PLLC

(57) **ABSTRACT**

An electrochemical deposition and testing system consisting of individually addressable electrode arrays, a fully automated deposition head, and a parallel screening apparatus is described. The system is capable of synthesizing and screening millions of new compositions at an unprecedented rate.

**16 Claims, 6 Drawing Sheets**

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| 54 | US 5486282 A | 10 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 55 | US 5459102 A | 23 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 56 | US 5440239 A | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 57 | US 5437733 A | 15 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 58 | US 5376587 A | 14 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 59 | US 5368711 A | 15 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |

Brief Summary Text - BSTX (6):
low contact resistance to previous and subsequent metallization steps

Brief Summary Text - BSTX (17):
Sputtered aluminum has electromigration and step coverage concerns. Electromigration is an atomic transport mechanism which allows metal atoms to move due to an applied direct current resulting in the formation of voids in a metal line. These voids can cause an increase in line resistance and ultimately the opening of a line (open circuit). Step coverage describes the ability of the metal to fill contact and via holes. This directly affects the ability of the metal to carry current into and out of the contacts and vias. Poor step coverage may lead to the failure (open circuit) of the metal in the hole.

Brief Summary Text - BSTX (18):
Subsequent processing (planarization and stacking vias on top of contacts) is also complicated by poor step coverage. Layering the aluminum with a more electromigration resistant metal or alloying the aluminum (forming new phases at the sensitive grain boundaries) are two approaches to reduce the probability of this failure mechanism. They are only partial solutions and introduce other problems such as complicating the metal etch step and increasing the sheet resistance of the metal. Solving the step coverage problem with standard sputtering techniques has also convincingly failed.

Detailed Description Text - DETX (63):
Referring back to FIG. 9, when the cathode (wafer) 5 is secured against the cathode gasket.cndot. 3, electrolyte is excluded from contacting the area of the wafer contacting this cathode gasket 3 as well as the cathode wires 4. The cathode wires 4 penetrate the photoresist (where present) on the active side of the wafer and make ohmic contact with the nucleating layer/diffusion barrier (this would be the top surface observed in FIG. 5). Four separate cathode wires 4 (A,B,C and D) are employed to allow the confirmation of good contact between the wafer and electrode wires (by making a resistance measurement) before electrolyte is introduced into the cell and electrodeposition is initiated. A knowledge of the diffusion barrier/nucleation layer sheet resistance along with the cell geometry will allow the determination of good cathode wire to cathode contact. Wires A and C may be checked followed by the resistance between wires B and D.

Claims Text - CLTX (11):
5. The apparatus as in claim 3 further including a second cathode wire for producing electrical contact to said nucleation layer, so that good ohmic contact of said cathode wires can be ascertained by a resistance check across said first and second cathode wires subsequent to loading said semiconductor in said apparatus and prior to introduction of electrolyte into said apparatus.

Current US Cross Reference Classification - CCXR (2):
205/123

# United States Patent [19]

Poris

[11] Patent Number: 5,368,711

[45] Date of Patent: Nov. 29, 1994

[54] SELECTIVE METAL ELECTRODEPOSITION PROCESS AND APPARATUS

[76] Inventor: Jaime Poris, 21955 Bear Creek Way, Los Gatos, Calif. 95030

[21] Appl. No.: 57,141

[22] Filed: Apr. 29, 1993

Related U.S. Application Data

[60] Division of Ser. No. 799,734, Nov. 22, 1991, Pat. No. 5,256,274, which is a continuation-in-part of Ser. No. 561,168, Aug. 1, 1990, abandoned.

[51] Int. Cl.[5] ........ C25D 5/02

[52] U.S. Cl. ........ 204/193; 205/118; 205/123

[58] Field of Search ........ 204/193; 205/118, 123

[56] References Cited

U.S. PATENT DOCUMENTS

4,927,505 5/1990 Sharma et al. ........ 204/34.5

Primary Examiner—John Niebling
Assistant Examiner—Kishor Mayekar
Attorney, Agent, or Firm—Heller, Ehrman, White & McAuliffe

[57] ABSTRACT

A process and apparatus for advanced semiconductor applications which involves the selective electrodeposition of metal on a semiconductor wafer is described. The present invention has significant economic and performance advantages over the current state of the art. It addresses problems associated with cleanliness (a major issue with sub-micron processing), metal thickness uniformity, step coverage and environmental concerns.

A metal with better device performance capabilities compared to the standard aluminum is also employed. The hardware allows the selective deposition to occur without allowing the electrolyte to contact the rear of the wafer or the electrodes contacting the front wafer surface. A virtual anode improves the primary current distribution improving the thickness uniformity while allowing optimization of other film parameters with the remaining deposition variables. Using this process and the associated hardware, metal lines are selectively deposited with contacts or vias completely filled without the need for plasma etching the deposited metal.

8 Claims, 7 Drawing Sheets

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| 53 | US 5503731 A | 15 | ☐ | | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 54 | US 5486282 A | 10 | ☐ | | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 55 | US 5459102 A | 23 | ☐ | | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 56 | US 5440239 A | 12 | ☐ | | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 57 | US 5437733 A | 15 | ☐ | | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 58 | US 5376587 A | 14 | ☐ | | ☐ | ☑ | ☐ | ☐ | | USPAT |
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Referring back to FIG. 9, when the cathode (wafer) 5 is secured against the cathode gasket.cndot. 3, electrolyte is excluded from contacting the area of the wafer contacting this cathode gasket 3 as well as the cathode wires 4. The cathode wires 4 penetrate the photoresist (where present) on the active side of the wafer and make ohmic contact with the nucleating layer/diffusion barrier (this would be the top surface observed in FIG. 5). Four separate cathode wires 4 (A,B,C and D) are employed to allow the confirmation of good contact between the wafer and electrode wires (by making a resistance measurement) before electrolyte is introduced into the cell and electrodeposition is initiated. A knowledge of the diffusion barrier/nucleation layer sheet resistance along with the cell geometry will allow the determination of good cathode wire to cathode contact. Wires A and C may be checked followed by the resistance between wires B and D.

Claims Text - CLTX (11):
5. The apparatus as in claim 3 further including a second cathode wire for producing electrical contact to said nucleation layer, so that good ohmic contact of said cathode wires can be ascertained by a resistance check across said first and second cathode wires subsequent to loading said semiconductor in said apparatus and prior to introduction of electrolyte into said apparatus.

Current US Cross Reference Classification - CCXR (2):
205/123



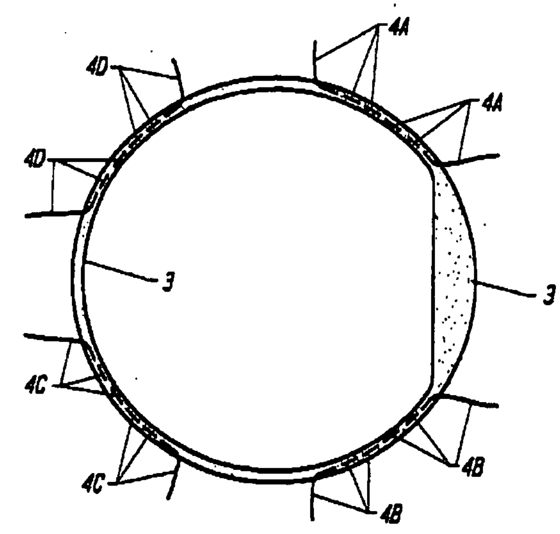


FIG. 10A

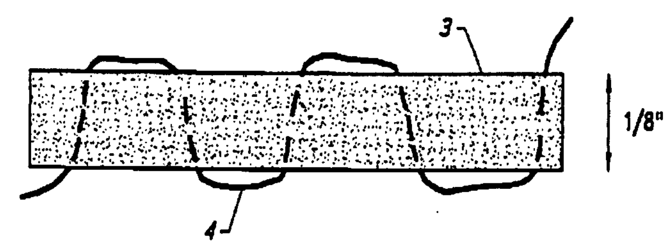


FIG. 10B

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| 93 | US 3653999 A | 6 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 94 | US 3620932 A | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 95 | US 20030168346 A | 46 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
| 96 | US 20030168345 A | 7 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |

PGPUB-DOCUMENT-NUMBER: 20030168345

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030168345 A1

TITLE: In-situ monitor seed for copper plating

PUBLICATION-DATE: September 11, 2003

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY | RULE-47 |
|---|---|---|---|---|
| Tsai, Minghsing | Hsin-Chu | | TW | |
| Chou, Shih-Wei | Taipei | | TW | |

ASSIGNEE-INFORMATION:

| NAME | CITY | STATE | COUNTRY | TYPE CODE |
|---|---|---|---|---|
| Taiwan Semiconductor Manufacturing Co., Ltd. | | | | 03 |

APPL-NO: 10/ 093177

DATE FILED: March 7, 2002

INT-CL: [07], C25D007/12

US-CL-PUBLISHED: 205/157

US-CL-CURRENT: 205/157

REFERENCE-FIGURES: 1

ABSTRACT:

A method and apparatus for monitoring copper seed layer growth during copper plating of a semiconductor wafer. A ring contact for use in copper plating of the semiconductor wafer is generally divided into a plurality of switches thereof. The ring contact is biased to prior to copper plating of the semiconductor wafer to determine a copper seed layer conductivity. Each switch among the plurality of switches can be connected together and thereafter the switches may be biased to an anode during copper plating, thereby permitting in-situ monitoring of copper seed resistance prior to the copper plating and a detection of copper seed damage and copper seed corrosion associated with the copper plating.

BRIEF SUMMARY:

TECHNICAL FIELD

[0001] The present invention relates generally to semiconductor fabrication techniques and devices. The present invention also relates to copper plating devices and techniques utilized in the fabrication of integrated circuits on semiconductor wafers. The present invention also relates to contact rings utilized in copper plating processes and devices.

BACKGROUND OF THE INVENTION

(19) United States
(12) Patent Application Publication (10) Pub. No.: US 2003/0168345 A1
Tsai et al. (43) Pub. Date: Sep. 11, 2003

(54) IN-SITU MONITOR SEED FOR COPPER PLATING

(75) Inventors: Minghsing Tsai, Hsin-Chu (TW); Shih-Wei Chou, Taipei (TW)

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(73) Assignee: Taiwan Semiconductor Manufacturing Co., Ltd.

(21) Appl. No.: 10/093,177

(22) Filed: Mar. 7, 2002

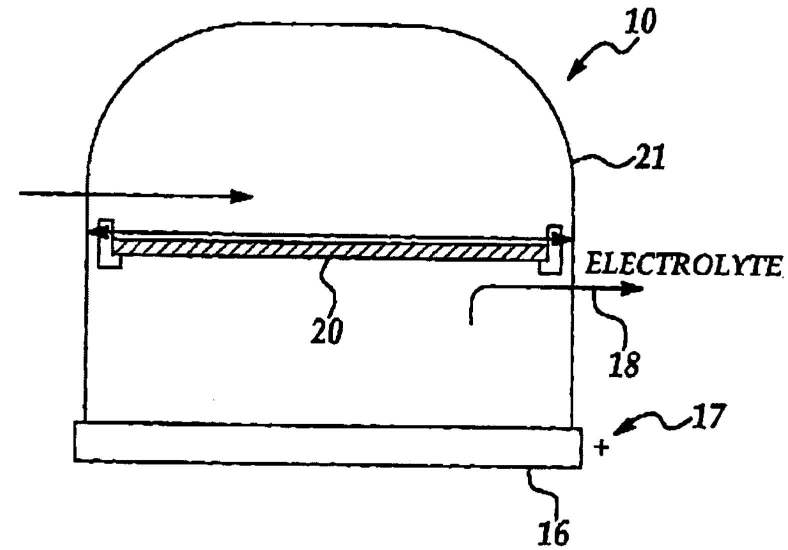
Publication Classification

(51) Int. Cl.[7] ..................... C25D 7/12

(52) U.S. Cl. ..................... 205/157

(57) ABSTRACT

A method and apparatus for monitoring copper seed layer growth during copper plating of a semiconductor wafer. A ring contact for use in copper plating of the semiconductor wafer is generally divided into a plurality of switches thereof. The ring contact is biased to prior to copper plating of the semiconductor wafer to determine a copper seed layer conductivity. Each switch among the plurality of switches can be connected together and thereafter the switches may be biased to an anode during copper plating, thereby permitting in-situ monitoring of copper seed resistance prior to the copper plating and a detection of copper seed damage and copper seed corrosion associated with the copper plating.

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| 103 | US 20020027081 A | 56 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
| 104 | US 20020027080 A | 51 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
| 105 | US 20020008036 A | 95 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
| 106 | US 20020000380 A | 43 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
| 107 | US 20010040098 A | 28 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |

release the airtight state of the plating chamber during wafer transferring, the mist in the plating chamber is scattered out of the plating chamber. Thus, in the conventional plating apparatus, there was a possibility that contamination caused by mist of plating solution was not sufficiently prevented, with the result that plating with high reliability was not performed.

[0009] Moreover, in the aforementioned plating apparatus, a processing object, for example, a semiconductor wafer is applied given voltage through a plurality of contact pins provided in a holding member for holding the processing object. Accordingly, there is a problem in which a nonuniform film is formed on the processing object or no plating is performed when electrical contact of contact pins to the processing object is poor.

[0010] As a method for checking the contact state of contact pins to the processing object, there is a method disclosed in Unexamined- Japanese Patent Application KOKAI Publication No. H11-181600. This is the method in which a resistance value between two contact pins connected to each other is measured by a resistance measuring device to confirm the contact state of contact pins from the resistance values.

[0011] The above method, however, is to confirm the contact state of the contact pins interposed between two contact pins. Accordingly, it is impossible to know which contact pin has contact failure. In order to check the contact state of each contact pin in detail, numerous resistance measuring devices must be used, and this makes the apparatus structure complicated. Thus, there was a possibility that the conventional plating apparatus did not confirm the passage of electric current through the processing object and the contact pins with ease and without fail, resulting that plating with high reliability was not performed.

SUMMARY OF THE INVENTION

[0012] With consideration given to the aforementioned problems, it is an object of the present invention to provide a processing apparatus and a processing system with high reliability.

[0013] Other object of the present invention is to provide a processing apparatus and a processing system with easy maintenance.

[0014] Another object of the present invention is to provide a processing apparatus and a processing system, which is capable of easy and sure checking of electrical contact state.

[0015] In order to attain the above objects, according to the present invention, there is provided a processing apparatus comprising a chamber having a first area for performing a delivery of a processing object between an outer section and the chamber, and a second area for providing given processing to the processing object; a process solution bath, provided in the second area, for reserving a process solution; a processing mechanism for providing predetermined processing to the processing object using the process solution in the second area; a sucking line, provided in the first area, for sucking atmosphere of the first area in the vicinity of a boundary between the first area and the second area; and an exhaust line, provided in the second area, for exhausting atmosphere in the second area to the outer section in the vicinity of the boundary between the first area and the second area.

(19) United States
(12) Patent Application Publication (10) Pub. No.: US 2001/0040098 A1
Okase et al. (43) Pub. Date: Nov. 15, 2001

(54) PROCESSING APPARATUS AND PROCESSING SYSTEM

(76) Inventors: Wataru Okase, Kanagawa (JP); Takenobu Matsuo, Kanagawa (JP)

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101 Broadway
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(21) Appl. No.: 09/846,660

(22) Filed: May 1, 2001

(30) Foreign Application Priority Data

May 2, 2000 (JP) .............................. 2000-133454
May 8, 2000 (JP) .............................. 2000-135207
May 8, 2000 (JP) .............................. 2000-135227

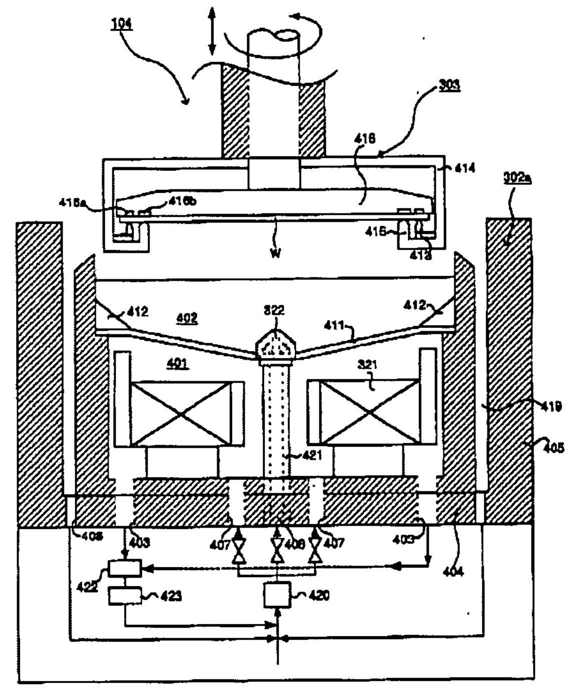
Publication Classification

(51) Int. Cl.7 .............. C25D 3/38; C25D 21/12; C25D 7/12; H01L 21/445; C25D 17/00; C25D 17/06

(52) U.S. Cl. .............. 205/82; 205/123; 204/199; 204/228.4; 204/228.6; 204/264

(57) ABSTRACT

A plating system is composed of a transfer device for performing transfer of a wafer, a plating unit and a washing/drying unit provided around the transfer device. Each unit is structured to be detachable from the plating system. The plating unit is divided into a wafer transfer section and a plating section by a separator, and atmosphere of each section is independently set.

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see ¶ 0093 measure resistance between contact pins
¶ 0088 measuring section 424b
claim 21, 30

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| 103 | US 20020027081 A | 56 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
| 104 | US 20020027080 A | 51 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
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| 106 | US 20020000380 A | 43 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |
| 107 | US 20010040098 A | 28 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | US-PG |

small current flows.

[0089] The measuring device 424 is connected to the controller 318. The measuring device 424 sends obtained current value data between each contact pin 413a and each probe 418 to the controller 318. The controller 318 determines the contact (connection) state of each contact pin 413a from the current quantities.

[0090] For example, the controller 318 determines that the contact state of contact pin 413a is normal when the current value between the contact pin 413a and the corresponding probe 418 is more than a predetermined value. While, in the case where the current value is below the predetermined value, the controller 318 determines that the contact state of contact pin 413a is abnormal.

[0091] The controller 318 performs control of the overall apparatus such as continuation of plating or stop processing, and the like based on the determination result. This makes it possible to check the contact state of each contact pin 413a without fail, and to perform plating with high reliability.

[0092] An explanation will be next given of a plating method using the above-structured plating unit 104. First, the contact state of contact pin 413a of the cathode electrode 413 is checked before the wafer W is plated. As illustrated in FIG. 9A, the pressing tool 416 rises in the holding section 414. At this time, the pressing tool 416, the contact pin 413a , and the seal section 415 are spaced one another.

[0093] Next, as illustrated in FIG. 9B, the pressing tool 416 moves down. At the position corresponding to the contact pin 413a of the lower surface of the pressing tool 416, the first concave portion 416a is formed. At the position corresponding to the seal section 415 of the lower surface of the pressing tool 416, the second concave portion 416b is formed. Accordingly, when the pressing tool 416 moves down, the contact pin 413a is contained in the first concave portion 416a and the seal section 415 is contained in the second concave portion 416b. At this time, the probe 418 in the first concave portion 416a and the contact pin 413a are in contact with each other. In this state, the measuring device 424 measures the electrical resistance between each pair of contact pin 413a of the cathode electrode 413 and probe 418 sequentially.

[0094] The controller 318 determines that the contact state of contact pin 413a is normal when the current value between the contact pin 413a and the corresponding probe 418 is more than a predetermined value. While, in the case where the current value is below the predetermined value, the controller 318 determines that the contact state of contact pin 413a is abnormal. The controller 318 stops plating when determining that the contact state is abnormal, and continues plating when determining the contact state is normal.

[0095] After checking contact (connection), the pressing tool 416 rises and a space is formed among the pressing tool 416, the contact pin 413a, and the seal section 415. Then, as illustrated in FIG. 9C, the second wafer transfer apparatus 213 loads the wafer W into the plating unit 104 through the space and mounts the wafer W on the contact pins 413a and the seal sections 415.

[0096] Sequentially, as illustrated in FIG. 9D, the pressing tool 416 moves down and presses the wafer W from the above. This fixes the wafer W to be adhered to the seal section 415. Next, the holding section 414 moves down as holding the state that the pressing tool 416 presses the wafer W, so that the

Patent Application Publication Nov. 15, 2001 Sheet 8 of 14 US 2001/0040098 A1

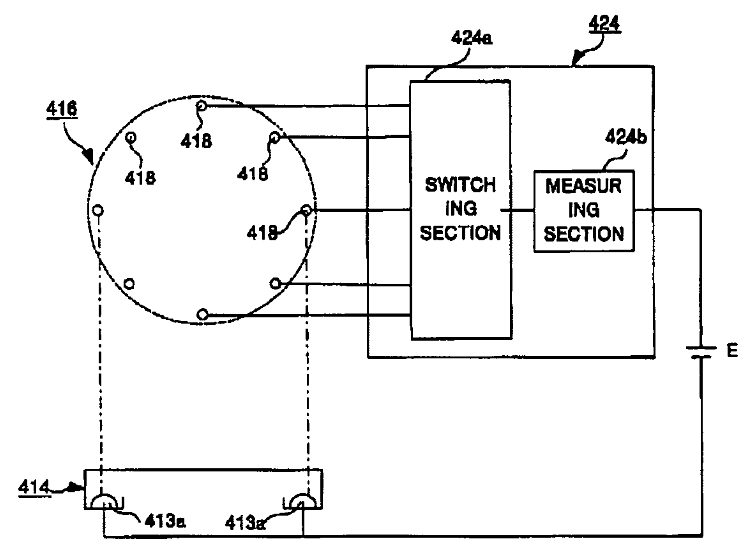


FIG.8

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- Pending
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  - L1: (609) ((205/123) or (205/157)).CCLS.
  - L2: (1479716) contact or contacts
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L2: (1479716) contact or contacts
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L8: (414681) measurement or measurment
L9: (1220894) 17 or 18
L10: (38669) 13 near3 19
L11: (17) 110 and 11
L12: (55525) 13 near10 19
L13: (22) 112 and 11
L14: (5) 113 not 111
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  - L7: (1171047) measure or measures or measured or measuring
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  - L9: (1220894) 17 or 18
  - L10: (38669) 13 near3 19
  - L11: (17) 110 and 11
  - L12: (55525) 13 near10 19
  - L13: (22) 112 and 11
  - L14: (5) 113 not 111
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| 1 | US 6544397 B2 | 5 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 2 | US 6444109 B1 | 5 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 3 | US 6322963 B1 | 25 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 4 | US 6200451 B1 | 5 | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 5 | US 6146515 A | 10 | ☐ | ☑ | ☐ | ☐ | | USPAT |
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| 7 | US 5739692 A | 9 | ☑ | ☐ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6146515

DOCUMENT-IDENTIFIER: US 6146515 A

TITLE: Power supply and method for producing non-periodic complex waveforms

---------- KWIC ---------

Detailed Description Text - DETX (23):

An optional process feedback system can be implemented to measure any plating variable, for instance, resistance barrier layers at the cathodic surface. Such information is fed back to the secondary rectification portion 330 in the form of a voltage or current signal. The output can then be modulated in proportion to the feedback signal and according to variables set by the user in order to compensate for plating process variables in a closed loop system. The user may view the feedback signal on the LCD display panel (or computer monitor), and set reference and factor parameters to determine the behavior of the system based on the equation:

Current US Original Classification - CCOR (1):
205/81

# United States Patent [19]

Gutiérrez et al.

[11] Patent Number: 6,146,515

[45] Date of Patent: Nov. 14, 2000

[54] POWER SUPPLY AND METHOD FOR PRODUCING NON-PERIODIC COMPLEX WAVEFORMS

[75] Inventors: Enrique Gutiérrez, Arlington Hts.; Bonifacio Diaz, Chicago, both of Ill.; Rogelio Valenzuela, Chihuahua, Mexico

[73] Assignee: Tecnu, Inc., Arlington Heights, Ill.

[21] Appl. No.: 09/212,939

[22] Filed: Dec. 16, 1998

[51] Int. Cl.$^7$ .................... C25D 21/12

[52] U.S. Cl. .................... 205/81; 204/229.5; 204/230.6

[58] Field of Search .................... 204/229.5, 230.6; 205/81

[56] References Cited

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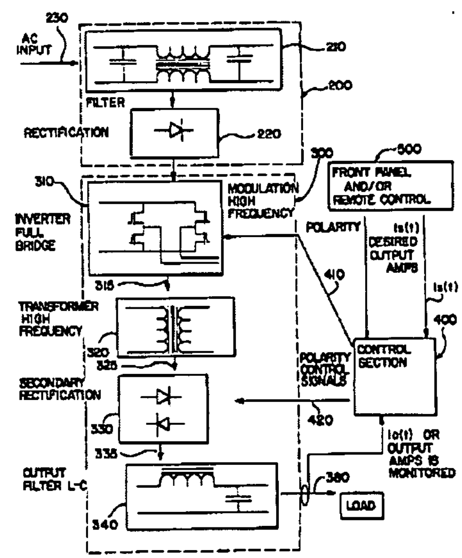
Primary Examiner—Kathryn Gorgos
Assistant Examiner—Thomas H. Parsons
Attorney, Agent, or Firm—Wallenstein & Wagner, Ltd.

[57] ABSTRACT

A power supply for producing complex non-periodic waveforms from a sum of periodic waveforms is disclosed. The power supply includes a controller which measures the output signal and compares it to the desired signal in order to produce an error signal. The error signal is fed to the power stage and is used to modify the input signal and produce the desired output. The desired signal is programmed by the user by selecting a plurality of pre-defined stored waveforms, modifying them, and arranging them such that the desired complex non-periodic waveform is created. The user can enter the instructions for modifying and arranging the waveforms via a panel having a keypad and display, or using a computer running software which enables the user to modify the stored waveforms on-screen. Such control is particularly useful in industries in which a very specific complex output signal is desirable, such as in the electrolytic plating industry. An optional process feedback system may be employed to monitor and respond to plating process variables.

22 Claims, 5 Drawing Sheets

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  - L1: (609) ((205/123) or (205/157)).CCLS.
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  - L4: (132389) l2 same l3
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  - L9: (1220894) l7 or l8
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  - L11: (17) l10 and l1
  - L12: (55525) l3 near10 l9
  - L13: (22) l12 and l1
  - L14: (5) l13 not l11
  - L15: (331) (205/81-85).CCLS.
  - L16: (28) l12 and l15
  - L17: (33) l4 and l15
  - L18: (27) l17 not l5
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L14: (5) l13 not l11
L15: (331) (205/81-85).CCLS.
L16: (28) l12 and l15
L17: (33) l4 and l15
L18: (27) l17 not l5
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| 1 | US RE37749 E | 15 | | USPAT |
| 2 | US 6613214 B2 | 28 | | USPAT |
| 3 | US 6585876 B2 | 47 | | USPAT |
| 4 | US 6582578 B1 | 54 | | USPAT |
| 5 | US 6576110 B2 | 35 | | USPAT |
| 6 | US 6572742 B1 | 30 | | USPAT |
| 7 | US 6444101 B1 | 15 | | USPAT |

US-PAT-NO: 6613214

DOCUMENT-IDENTIFIER: US 6613214 B2

TITLE: Electric contact element for electrochemical deposition system and method

---------- KWIC ---------

Detailed Description Text - DETX (15):

Although the electric contact ring 152 of the present invention is designed to resist deposit buildup on the inner electric contact elements 172, over multiple substrate plating cycles the substrate-electric contact element interface resistance may increase, eventually reaching an unacceptable value. An electronic sensor/alarm 204 can be connected across the external resistor 200 to monitor the voltage/current across the external resistor to address this problem. If the voltage/current across the external resistor 200 falls outside of a preset operating range that is indicative of a high substrate-electric contact element resistance, the sensor/alarm 204 triggers corrective measures such as shutting down the plating process until the problems are corrected by an operator. Alternatively, a separate controller can be connected to each electric contact element 165 and can be separately controlled and monitored to provide a uniform current distribution across the substrate. A very smart system (VSS) may also be used to modulate the current flow. The VSS typically comprises a processing unit and any combination of devices known in the industry used to supply and/or control current such as variable resistors, separate controllers, etc. As the physiochemical, and hence electrical, properties of the inner electric contact elements 172 change over time, the VSS processes and analyzes data feedback. The data is compared to pre-established setpoints and the VSS then makes appropriate current and voltage alterations to ensure uniform deposition.

Current US Cross Reference Classification - CCXR (2):
204/224R

(12) **United States Patent**
Dordi et al.

(10) Patent No.: **US 6,613,214 B2**
(45) Date of Patent: **Sep. 2, 2003**

(54) **ELECTRIC CONTACT ELEMENT FOR ELECTROCHEMICAL DEPOSITION SYSTEM AND METHOD**

(75) Inventors: **Yezdi N. Dordi**, Palo Alto, CA (US); **Joseph J. Stevens**, San Jose, CA (US)

(73) Assignee: **Applied Materials, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 96 days.

(21) Appl. No.: 09/730,968

(22) Filed: Dec. 5, 2000

(65) **Prior Publication Data**

US 2001/0000396 A1 Apr. 26, 2001

**Related U.S. Application Data**

(63) Continuation-in-part of application No. 09/289,074, filed on Apr. 8, 1999, now Pat. No. 6,258,220, which is a continuation-in-part of application No. 09/201,486, filed on Nov. 30, 1998, now Pat. No. 6,251,236.

(51) Int. Cl.⁷ .......................... C25D 5/02; C25D 5/00; C25D 17/00

(52) U.S. Cl. ...................... 205/118; 205/137; 204/212; 204/224 R; 204/297.01

(58) Field of Search .......................... 204/297.01, 212, 204/224 R; 205/118, 137

(56) **References Cited**

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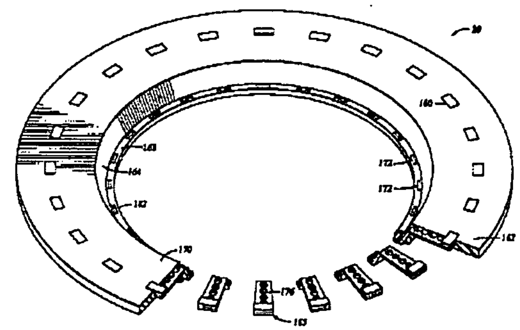
(List continued on next page.)

*Primary Examiner*—Donald R. Valentine
(74) *Attorney, Agent, or Firm*—Moser, Patterson & Sheridan

(57) **ABSTRACT**

An apparatus and associated method for deposition of metal ions contained in an electrolyte solution to form a metal film primarily on a seed layer formed on at least a first side of a substrate. The substrate has a second side that is opposed the first side and an edge joining the first side and the second side. The apparatus comprises a substrate holder system and an electric contact element. The electric contact element physically contacts one of the second side or the edge of the substrate. In one aspect, the substrate is rotated about its vertical axis when the seed layer of substrate is immersed in the electrolyte solution during the metal film deposition. In another aspect, the substrate is not rotated about its vertical axis when the seed layer on the substrate is immersed in the electrolyte solution during the metal film deposition. In different embodiments, the electric contact element contacts the seed layer on the second side of the substrate, a diffusion barrier layer on the second side of the substrate, or the seed layer on the edge of the substrate.

**38 Claims, 12 Drawing Sheets**



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L17: (33) l4 and l15
L18: (27) l17 not l5
L19: (780) (204/224R).CCLS.
L20: (17) l12 and l19
L21: (16) l20 not (l13 or l16)
L22: (1174) (204/228.1-230.8).CCLS.
L23: (57) l12 and l22
L24: (48) l23 not (l13 or l16 or l20)
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DBs: USPAT; US-PGPUB

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| 1 | US 6551484 B2 | 46 | | | | | | | ☑ | | | | USPAT |
| 2 | US 6517689 B1 | 23 | | | | | | | ☑ | | | | USPAT |
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| 7 | US 6267855 B1 | 31 | | | | | | ☑ | | | | | USPAT |

US-PAT-NO: 6517689

DOCUMENT-IDENTIFIER: US 6517689 B1
**See image for Certificate of Correction**

TITLE: Plating device

---------- KWIC ---------

Brief Summary Text - BSTX (17):
Further, it is preferable that the conduction detection device be provided with a contact resistance measuring device to measure contact resistance between a conductive layer on the plating surface of the substrate and individual feeding contacts so as to determine electrical conductivity properties of respective feeding contacts according to respective values of contact resistance measured by the contact resistance measuring device.

Drawing Description Text - DRTX (9):
FIG. 8 is a circuit diagram of a basic resistance measuring device to measure the resistance between the feeding contacts.

Drawing Description Text - DRTX (11):
FIG. 10 is a schematic wiring diagram of the circuits for contact resistance measuring and plating feeding for feeding contacts of the plating apparatus.

Drawing Description Text - DRTX (12):
FIG. 11 is a schematic circuit diagram of the contact resistance measuring device.

Detailed Description Text - DETX (9):
A method for checking the conduction state between the conductive layer of the substrate 12 and the feeding contact 15 is to measure the resistance value between two feeding contacts 15. The resistance value between two feeding contacts 15 is a combined resistance value R0 which comprises of the contact resistances R1 and R3 between the substrate 12 and the respective feeding contacts 15, and the resistance R2 of the conductive layer itself on the substrate 12. Here, values of the contact resistances R1, R3 are only about several hundred milli-ohms(m.OMEGA.), therefore, measurements must be performed with precision.

Detailed Description Text - DETX (15):
The combined resistance R0=R1+R2+R3 is usually in a range of 700.about.900 m.OMEGA. and to measure this low level of resistance accurately, it is necessary to cancel out the wire resistance. FIG. 9 shows an equivalent circuit for explaining the method for canceling the wire resistance. In FIG. 9, r1, r2 show the resistance values of the wiring connecting the constant current circuit 32 to each of the feeding contacts 15, 15 (A, B). And r3, r4 show the resistance values of wiring connecting the amplifier 33 to each of the feeding contacts 15, 15 (A, B) The current flowing in the constant current circuit 32 is designated by I.sub.M, the current flowing in the amplifier 33 by

(12) **United States Patent**
**Hongo et al.**

(10) Patent No.: **US 6,517,689 B1**
(45) Date of Patent: **Feb. 11, 2003**

(54) **PLATING DEVICE**

(75) Inventors: **Akihisa Hongo**, Tokyo (JP); **Kenichi Suzuki**, Tokyo (JP); **Atsushi Chono**, Tokyo (JP); **Mitsuo Tada**, Tokyo (JP); **Akira Ogata**, Tokyo (JP); **Satoshi Sendai**, Tokyo (JP); **Koji Mishima**, Tokyo (JP)

(73) Assignee: **Ebara Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/463,019**

(22) PCT Filed: **Jul. 9, 1999**

(86) PCT No.: **PCT/JP99/03729**

§ 371 (c)(1), (2), (4) Date: **Jan. 19, 2000**

(87) PCT Pub. No.: **WO00/03074**

PCT Pub. Date: **Jan. 20, 2000**

(30) **Foreign Application Priority Data**

Jul. 10, 1998 (JP) .................................... 10-195932
Jul. 16, 1998 (JP) .................................... 10-202270

(51) Int. Cl.⁷ .......................... **B23H 3/02**; B23H 7/04; B23H 7/14; C25B 15/00; C25B 9/00

(52) U.S. Cl. .......................... **204/228.7**; 204/229.8; 204/297.14

(58) Field of Search .......................... 204/229.8, 230.8, 204/228.1, 224 R, 297.05, 297.14, 228.7; 205/133

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6,071,399 A * 6/2000 Van der Bergen et al. .. 205/337
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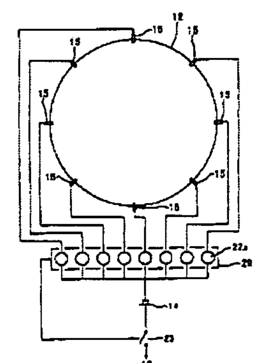
*Primary Examiner*—Nam Nguyen
*Assistant Examiner*—Wesley A. Nicolas
(74) *Attorney, Agent, or Firm*—Wenderoth, Lind & Ponack, L.L.P.

(57) **ABSTRACT**

The present invention is to provide a conduction detection device that can detect electrical conductivity (contact condition) of feeding contacts with conductive layers of a substrate. The present invention also provides an electroplating apparatus, which is able to produce uniform currents to flow through each of feeding contacts. The apparatus has a plating vessel, in which an electrode is disposed opposite to a substrate which is affixed to a plating jig electrically through a plurality of feeding contacts for applying a specific voltage between the electrode and conductive layers provided on a plating surface of the substrate. Plating current flows from the plating jig through the feeding contacts to the substrate. A conduction detection device is provided to detect electrical conductive states between the plurality of feeding contacts and the conductive layer on the substrate.

**29 Claims, 12 Drawing Sheets**

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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | US 6551484 B2 | 46 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 2 | US 6517689 B1 | 22 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 3 | US 6500317 B1 | 17 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 4 | US 6447668 B1 | 107 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 5 | US 6428681 B1 | 9 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 6 | US 6413389 B1 | 19 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 7 | US 6267855 B1 | 31 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6500317

DOCUMENT-IDENTIFIER: US 6500317 B1

TITLE: Plating apparatus for detecting the conductivity between plating contacts on a substrate

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Brief Summary Text - BSTX (9):
To solve the above mentioned subject matter, there is provided a method for confirming conductivity state between a plating jig having a plurality of conducting pins and a substrate to be plated having a conductive film, the substrate being mounted on the plating jig having a plurality of conducting pins such that the conducting pins contact the conductive film thereon, the method comprising: disposing the conducting pins of the plating jig being electrically separated independently with each other; attaching an end of reverse-current blocking diode to wiring connecting to the conducting pins, and connecting to the other ends of the reverse-current blocking diodes together to wiring connecting to a plating power source; and measuring an electrical resistance between the wiring so as to measure the electrical resistance between conducting pins of the plating jig.

Brief Summary Text - BSTX (10):
According to another aspect of the present invention, the conductivity state detector may comprise a contact resistance measuring device for measuring contact resistance between the feeder contacts and the conductive area on the surface of the substrate and detects the conductivity state of the feeder contacts based on the contact resistance measured by the contact resistance measuring device.

Drawing Description Text - DRTX (10):
FIG. 9 shows an example of a basic circuit construction for measuring resistance values between feeder contacts;

Drawing Description Text - DRTX (12):
FIG. 11 shows the wiring configuration for measuring contact resistance at the feeder contacts and supplying current for plating;

Drawing Description Text - DRTX (13):
FIG. 12 shows an example circuit construction for a contact resistance measuring device disposed at the feeder contacts; and

Detailed Description Text - DETX (5):
A resistance measuring device 4-1 is connected between the wires 3-1 and 3-3. A resistance measuring device 4-2 is connected between the wires 3-2 and 3-4. A jig having the circuit configuration described above is disposed opposite the anode 13 in the plating solution Q contained in the plating bath 10 shown in FIG. 1. The jig conducts electric current supplied from the DC power source (plating power source) 14. When each of the conducting pins 2-1,

(12) United States Patent
Yoshioka et al.

(10) Patent No.: US 6,500,317 B1
(45) Date of Patent: Dec. 31, 2002

(54) PLATING APPARATUS FOR DETECTING THE CONDUCTIVITY BETWEEN PLATING CONTACTS ON A SUBSTRATE

(75) Inventors: Junichiro Yoshioka; Satoshi Sendai; Atsushi Chono; Mitsuo Tada; Akihisa Hongo; Yoshitaka Mukaiyama; Kenya Tomioka; Akira Ogata; Kenichi Suzuki, all of Tokyo; Naomitsu Ozawa, Kanagawa, all of (JP)

(73) Assignee: Ebara Corporation, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/581,761

(22) PCT Filed: Dec. 16, 1998

(86) PCT No.: PCT/JP98/05672

§ 371 (c)(1),
(2), (4) Date: Jun. 16, 2000

(87) PCT Pub. No.: WO99/31304

PCT Pub. Date: Jun. 24, 1999

(30) Foreign Application Priority Data

Dec. 16, 1997 (JP) .......... 9-363944
Jul. 10, 1998 (JP) .......... 10-195932

(51) Int. Cl.[7] .......... C25B 9/04; C25D 21/12
(52) U.S. Cl. .......... 204/228.7; 204/229.8; 204/230.8

(58) Field of Search .......... 204/229.8, 230.8, 204/228.1, 224 R, 297.05, 297.14, 228.7; 205/133

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6,139,712 A 10/2000 Patton et al.
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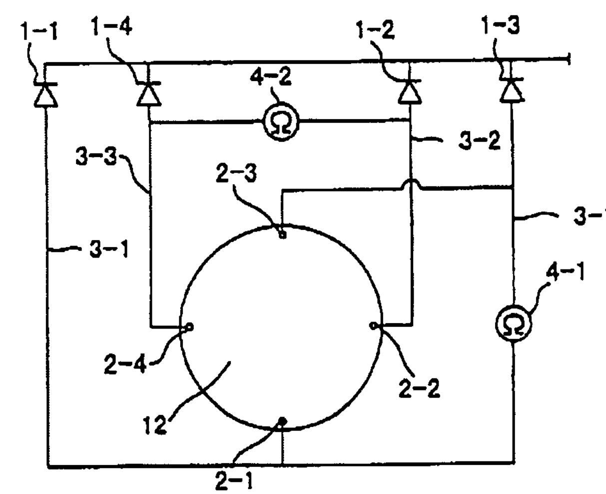
Primary Examiner—Nam Nguyen
Assistant Examiner—Wesley A. Nicolas
(74) Attorney, Agent, or Firm—Wenderoth, Lind & Ponack, L.L.P.

(57) ABSTRACT

The present invention provides a conductivity sensing device capable of detecting the conductivity (contact state) of the plurality of feeder contacts contacting the conductive area of the substrate, and a plating apparatus capable of forming a plating film of uniform thickness by supplying a uniform plating current through a plurality of feeder contacts.

5 Claims, 12 Drawing Sheets

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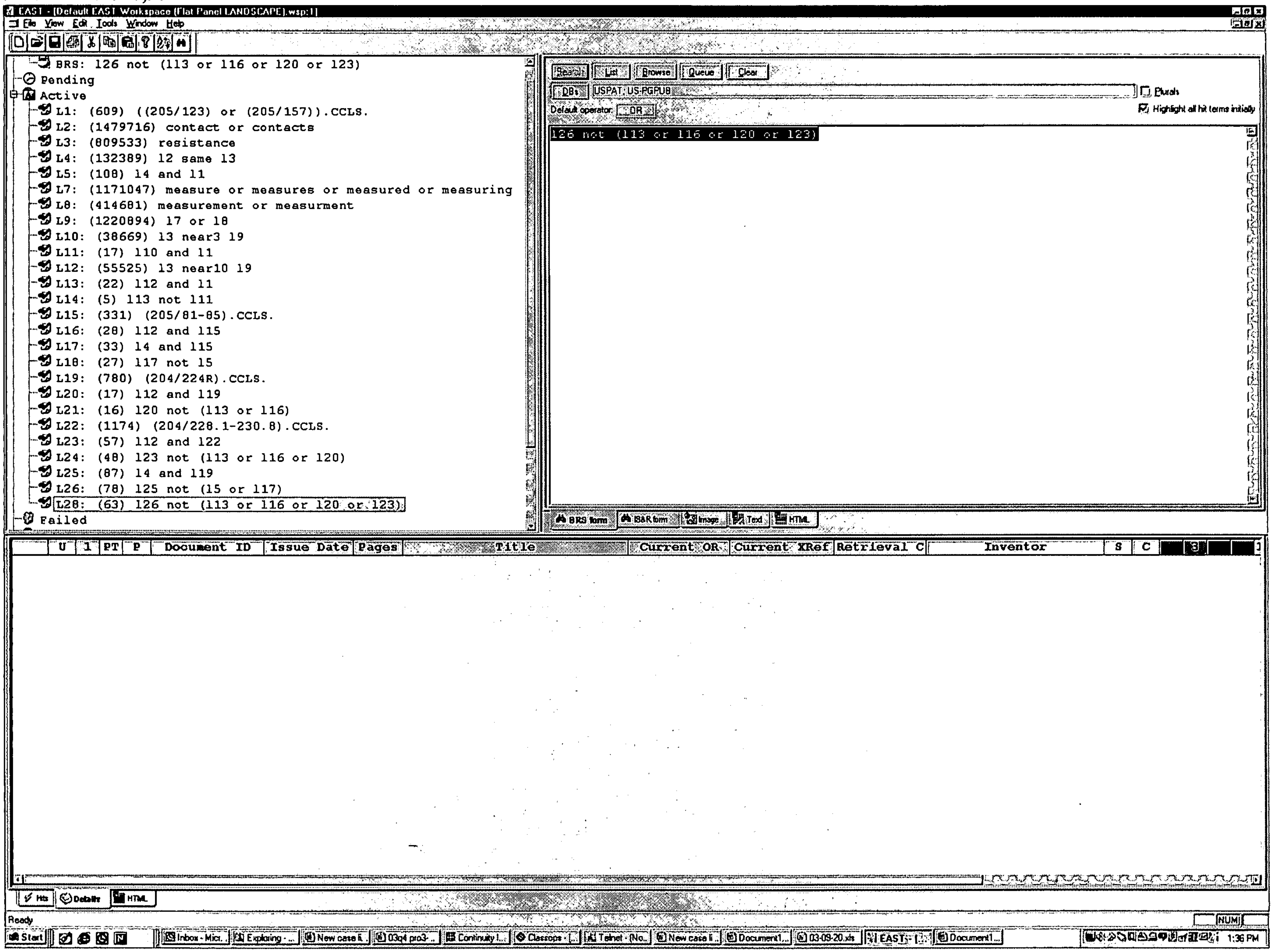

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Active
- L1: (609) ((205/123) or (205/157)).CCLS.
- L2: (1479716) contact or contacts
- L3: (809533) resistance
- L4: (132389) l2 same l3
- L5: (108) l4 and l1
- L7: (1171047) measure or measures or measured or measuring
- L8: (414681) measurement or measurment
- L9: (1220894) l7 or l8
- L10: (38669) l3 near3 l9
- L11: (17) l10 and l1
- L12: (55525) l3 near10 l9
- L13: (22) l12 and l1
- L14: (5) l13 not l11
- L15: (331) (205/81-85).CCLS.
- L16: (28) l12 and l15
- L17: (33) l4 and l15
- L18: (27) l17 not l5
- L19: (780) (204/224R).CCLS.
- L20: (17) l12 and l19
- L21: (16) l20 not (l13 or l16)
- L22: (1174) (204/228.1-230.8).CCLS.
- L23: (57) l12 and l22
- L24: (48) l23 not (l13 or l16 or l20)
- L25: (87) l4 and l19
- L26: (78) l25 not (l5 or l17)
- L28: (63) l26 not (l13 or l16 or l20 or l23)
- L29: (94) l4 and l22
- L30: (75) l29 not (l5 or l17 or l25)
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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | US 6524464 B2 | 9 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☒ | ☐ | ☐ | | USPAT |
| 2 | US 6436270 B1 | 5 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☒ | ☐ | ☐ | | USPAT |
| 3 | US 6432282 B1 | 11 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☒ | ☐ | ☐ | | USPAT |
| 4 | US 6428689 B1 | 25 | ☐ | ☐ | ☐ | ☐ | ☐ | ☒ | ☐ | ☐ | ☐ | | USPAT |
| 5 | US 6361678 B1 | 15 | ☐ | ☐ | ☐ | ☐ | ☐ | ☒ | ☐ | ☐ | ☐ | | USPAT |
| 6 | US 6337002 B1 | 11 | ☐ | ☐ | ☐ | ☐ | ☐ | ☒ | ☐ | ☐ | ☐ | | USPAT |
| 7 | US 6267860 B1 | 12 | ☐ | ☐ | ☐ | ☐ | ☐ | ☒ | ☐ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6432282

DOCUMENT-IDENTIFIER: US 6432282 B1
**See image for Certificate of Correction**

TITLE: Method and apparatus for supplying electricity uniformly to a workpiece

---------- KWIC ---------

Brief Summary Text - BSTX (9):
In metal deposition systems, several things may lend to uneven depositing of the metal layer. One major contributor to a non-uniform deposition of process time dependent variations in material buildup upon the different contacts 56. Each contact will thus develop unique and unpredictable geometric profiles and densities, thus producing varying and unpredictable resistances when exposed to a similar voltage. The varying resistance of the individual contacts 56 results in a non-uniform current density distribution across the wafer. The varying resistances of the contacts provide modified electrical fields. In addition, the contact resistance at the contact/seed layer interface may vary from wafer 48 to wafer, resulting in inconsistent plating distribution between different wafers using the same equipment.

Brief Summary Text - BSTX (10):
The power supply circuit that supplies current to the seed layer includes the plurality of contacts 56 located on a contact ring. In electroplater embodiments, a single power supply applies electricity to a junction that is electrically connected to all of the metal contacts 56. The electrical characteristics of different contacts may vary, especially after prolonged use. Those metal contacts having a higher resistance provide less electrical current to the adjacent seed layer. If an equal voltage is applied to each metal contact, these contacts with increased resistance also have a higher current flowing therethrough as indicated by Ohm's law. Non-uniform power distribution and current desities are applied to the seed layer across the wafer plating surface as a result of the varied electrical current applied by the contacts. This inequality of non-uniform power distribution and current densities results in uneven deposition of metal to the seed layer.

Detailed Description Text - DETX (8):
FIG. 2 depicts a power supply 22 of one embodiment of the present invention associated with fountain plater 10. This embodiment provides a design for the power supply that supplies power to individual contacts in which the electric currents supplied among the different contacts 56 are balanced even if the resistance of each contact 56 differs. The power supply 22 provides a more uniform electric current density (and application of electric current density) to the seed layer, even in those instances that contacts 56 have unequal resistances. An individual conductor with feedback portion 242 connects each contact 56 individually to a controller 204. Each individual conductor with feedback portion 242 senses the electric current being applied to its particular contact 56, and provides input to the controller 204 indicative of the electric current. The controller relies upon this sensed electrical current to balance the electric current between the different contacts 56 (if necessary), as described below.

(12) **United States Patent**
Shamouilian et al.

(10) Patent No.: **US 6,432,282 B1**
(45) Date of Patent: **Aug. 13, 2002**

(54) **METHOD AND APPARATUS FOR SUPPLYING ELECTRICITY UNIFORMLY TO A WORKPIECE**

(75) Inventors: Shamouil Shamouilian, San Jose; Anada H. Kumar, Milpitas; Donald J. Olgado, Palo Alto; Joseph J. Stevens, San Jose; Ricardo Leon, Palo Alto; Jon Clinton, San Jose, all of CA (US)

(73) Assignee: Applied Materials, Inc., Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/518,182

(22) Filed: Mar. 2, 2000

(51) Int. Cl.[7] ........ B23H 7/04; B23H 7/14; C25B 9/04

(52) U.S. Cl. ........ 204/228.1; 204/229.8; 204/230.2; 204/230.8; 204/286.1

(58) Field of Search ........ 204/229.8, 230.2, 204/286.1, 230.8, 224 R, 228.1

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WO WO 99/25905 5/1999 ........ C25D/5/02

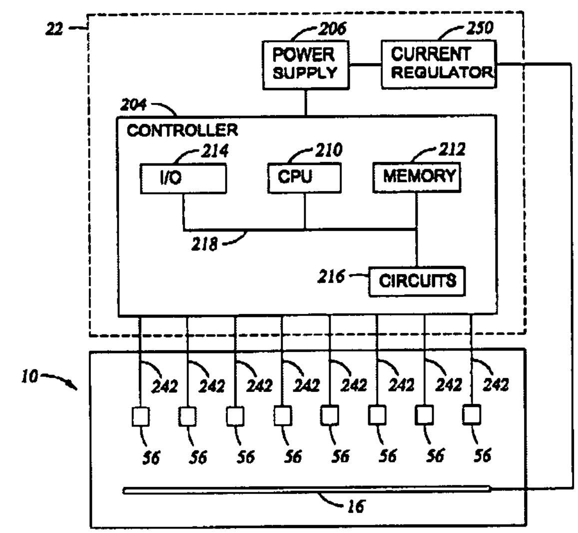
* cited by examiner

Primary Examiner—Robert Dawson
Assistant Examiner—Michael J Feely
(74) Attorney, Agent, or Firm—Moser, Patterson & Sheridan, LLP

(57) **ABSTRACT**

The present invention relates to a device that supplies electricity to a substrate. In one embodiment, the device includes multiple contacts, a current sensor, and a current regulator. The current sensor is attached to each of the plurality of contacts to sense their electric current. A current regulator controls current applied to each of the multiple contacts in response to the current sensor. In another embodiment, a compliant ridge is formed about the periphery of each contact to seal the contact from undesired chemicals.

11 Claims, 5 Drawing Sheets

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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | US 6599402 B2 | 25 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 2 | US 6585876 B2 | 47 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 3 | US 6582578 B1 | 54 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 4 | US 6576110 B2 | 35 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 5 | US 6551484 B2 | 46 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 6 | US 6416647 B1 | 28 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 7 | US 6241868 B1 | 9 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6576110

DOCUMENT-IDENTIFIER: US 6576110 B2

TITLE: Coated anode apparatus and associated method

---------- KWIC ---------

Detailed Description Text - DETX (22):
The conducting members 765 are defined by a plurality of outer electrical contact pads 780 annularly disposed on the flange 762, a plurality of inner electrical contact pads 772 disposed on a portion of the substrate seating surface 768, and a plurality of embedded conducting connectors 776 which link the pads 772, 780 to one another. The conducting members 765 are isolated from one another by the insulative body 770. The insulative body may be made of a plastic such as polyvinylidenefluoride (PVDF), perfluoroalkoxy resin (PFA), TEFLON.RTM. (a registered trademark of the E.I. duPont de Nemours and Company) and TEFZEL.RTM. (a registered trademark of the E.I. duPont de Nemours and Company) or any other insulating material such as Alumina (Al.sub.2 O.sub.3) or other ceramics. The outer contact pads 780 are coupled to a power supply, not shown, to deliver current and voltage to the inner contact pads 772 via the connectors 776 during processing. In turn, the inner contact pads 772 supply the current and voltage to a substrate by maintaining contact around a peripheral portion of the substrate. Thus, in operation the conducting members 765 act as discrete current paths electrically connected to a substrate.

Detailed Description Text - DETX (29):
FIG. 9 is a perspective view of an alternative embodiment of a cathode contact ring 1800. The cathode contact ring 1800 comprises a conductive metal or a metal alloy, such as stainless steel, copper, silver, gold, platinum, titanium, tantalum, and other conductive materials, or a combination of conductive materials, such as stainless steel coated with platinum. The cathode contact ring 1800 includes an upper mounting portion 1810 adapted for mounting the cathode contact ring onto the substrate holder assembly and a lower substrate receiving portion 1820 adapted for receiving a substrate therein. The substrate receiving portion 1820 includes an annular substrate seating surface 1822 having a plurality of contact pads or bumps 1824 disposed thereon and preferably evenly spaced apart. When a substrate is positioned on the substrate seating surface 1822, the contact pads 1824 physically contact a peripheral region of the substrate to provide electrical contact to the electroplating seed layer on the substrate deposition surface. Preferably, the contact pads 1824 are coated with a noble metal, such as platinum or gold, that is resistant to oxidation.

Current US Original Classification - CCOR (1):
205/89

Current US Cross Reference Classification - CCXR (12):
205/102

Current US Cross Reference Classification - CCXR (13):

U.S. Patent Jun. 10, 2003 Sheet 5 of 18 US 6,576,110 B2

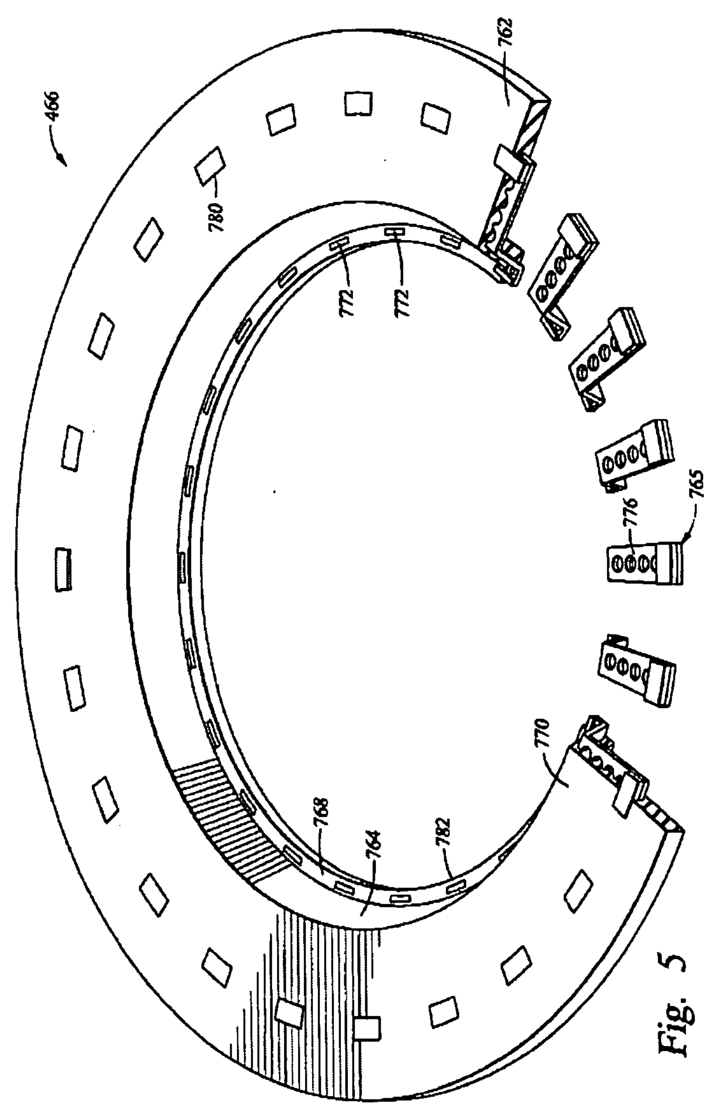


Fig. 5

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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | US 6572742 B1 | 30 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 2 | US 6547937 B1 | 26 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 3 | US 6475369 B1 | 30 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 4 | US 6444111 B1 | 62 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 5 | US 6436249 B1 | 64 | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | | USPAT |
| 6 | US 6379521 B1 | 25 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |
| 7 | US 6355153 B1 | 24 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6436249

DOCUMENT-IDENTIFIER: US 6436249 B1

TITLE: Clamshell apparatus for electrochemically treating semiconductor wafers

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Abstract Text - ABTX (1):
An apparatus for electroplating a wafer surface includes a cup having a central aperture defined by an inner perimeter, a compliant seal adjacent the inner perimeter, contacts adjacent the compliant seal and a cone attached to a rotatable spindle. The compliant seal forms a seal with the perimeter region of the wafer surface preventing plating solution from contaminating the wafer edge, wafer backside and the contacts. As a further measure to prevent contamination, the region behind the compliant seal is pressurized. By rotating the wafer during electroplating, bubble entrapment on the wafer surface is prevented. Further, the contacts can be arranged into banks of contacts and the resistivity between banks can be tested to detect poor electrical connections between the contacts and the wafer surface.

TITLE - TI (1):
Clamshell apparatus for electrochemically treating semiconductor wafers

Assistant Examiner - XA (1):
Smith-Hicks; Erica

Brief Summary Text - BSTX (2):
The present invention relates generally to a method and apparatus for treating the surface of a substrate and more particularly to a method and apparatus for electroplating a layer on a semiconductor wafer.

Brief Summary Text - BSTX (4):
The manufacture of semiconductor devices requires the formation of electrical conductors on semiconductor wafers. For example, electrically conductive leads on the wafer are often formed by electroplating (depositing) an electrically conductive material such as copper on the wafer and into patterned trenches.

Brief Summary Text - BSTX (5):
Electroplating involves making electrical contact with the wafer surface upon which the electrically conductive material is to be deposited (hereinafter the "wafer plating surface"). To insure a uniform deposition, it is important that the electrical contact with-the wafer plating surface be uniform and reliable.

Brief Summary Text - BSTX (6):
Brogden et al., U.S. Pat. No. 5,227,041 (hereinafter Brogden), teaches a

(12) **United States Patent**
Patton et al.

(10) Patent No.: **US 6,436,249 B1**
(45) Date of Patent: ***Aug. 20, 2002**

(54) **CLAMSHELL APPARATUS FOR ELECTROCHEMICALLY TREATING SEMICONDUCTOR WAFERS**


(75) Inventors: Evan E. Patton, Portland; Wayne Fetters, Canby, both of OR (US)

(73) Assignee: Novellus Systems, Inc., San Jose, CA (US)


(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.


(21) Appl. No.: 09/576,843

(22) Filed: May 17, 2000

**Related U.S. Application Data**

(63) Continuation of application No. 08/969,984, filed on Nov. 13, 1997, now Pat. No. 6,156,167.

(51) Int. Cl.[7] .......................... C25D 17/00; C25C 7/00; C25B 9/00

(52) U.S. Cl. .................................... 204/212; 204/270

(58) Field of Search ............................... 204/212, 270



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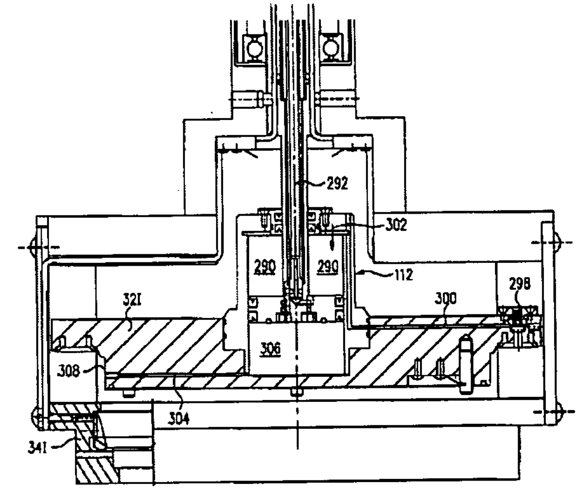
*Primary Examiner*—Donald R. Valentine
*Assistant Examiner*—Erica Smith-Hicks
(74) *Attorney, Agent, or Firm*—Skjerven Morrill LLP; Philip W. Woo


(57) **ABSTRACT**

An apparatus for electroplating a wafer surface includes a cup having a central aperture defined by an inner perimeter, a compliant seal adjacent the inner perimeter, contacts adjacent the compliant seal and a cone attached to a rotatable spindle. The compliant seal forms a seal with the perimeter region of the wafer surface preventing plating solution from contaminating the wafer edge, wafer backside and the contacts. As a further measure to prevent contamination, the region behind the compliant seal is pressurized. By rotating the wafer during electroplating, bubble entrapment on the wafer surface is prevented. Further, the contacts can be arranged into banks of contacts and the resistivity between banks can be tested to detect poor electrical connections between the contacts and the wafer surface.


**11 Claims, 48 Drawing Sheets**

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| 7 | US 6355153 B1 | 24 | ☐ | ☐ | ☐ | ☐ | ☐ | ☑ | ☐ | ☐ | ☐ | | USPAT |

US-PAT-NO: 6436249

DOCUMENT-IDENTIFIER: US 6436249 B1

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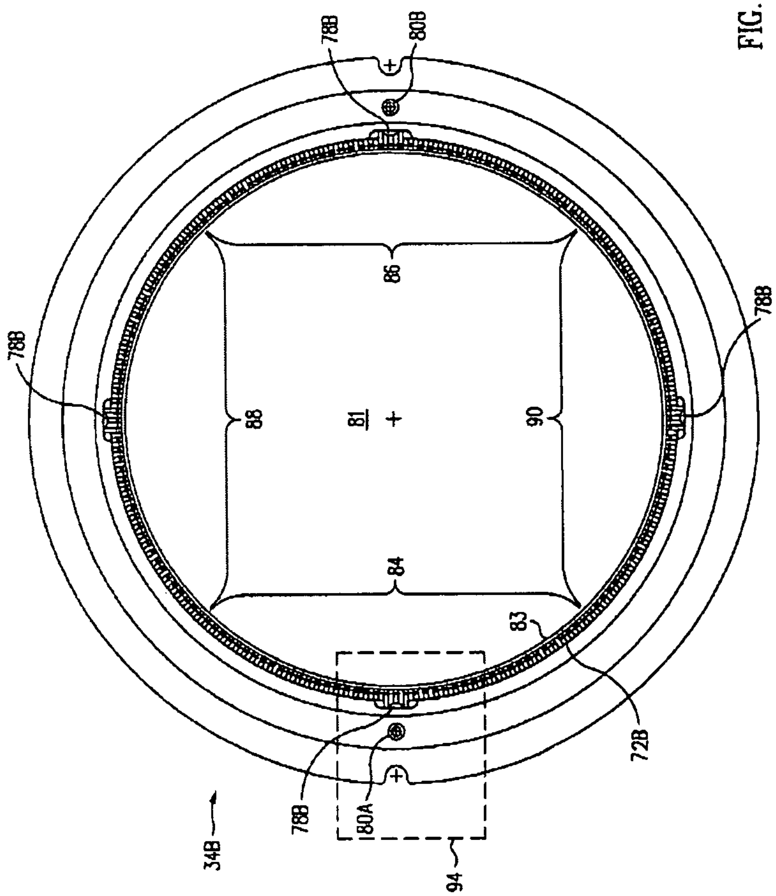


FIG. 10

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